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Impact of MOS Capacitor on Junctionless Double-Gate Field Effect Transistors a Visual TCAD Simulation Study

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ABSTRACT

Here we investigate the impact of MOS Capacitor on Junctionless Double-Gate Field Effect Transistors (DG JLFET) with the help of the Visual TCAD Simulations. The gate capacitance characteristics and the behavior with variations of applied gate and drain voltages of the Junctionless Accumulation Mode (JAM) devices are analyzed with different channel doping concentrations. The results obtained show us that increasing channel doping reduces gate capacitance due to the relocation of the charge centroid toward the center of the silicon body. Although intrinsic switching delay of a transistor in a circuit gets lowered with capacitance, excessive doping degrades mobility and drive current. The study highlights the trade-off between reduction in gate capacitance and current-driving capability of DG JLFET and provides essential design guidelines for future nanoscale junctionless transistors.

Keywords: MOS Capacitor; Gate Capacitance; Channel Doping Concentration; Junctionless Transistor; Double-Gate FET; Switching Delay; Electrostatic Control; Charge Distribution; Nanoscale Transistors; TCAD Simulation; Semiconductor Device Modelling.

1. Introduction

The advancement of modern integrated circuits is mainly attribute by the continuous reduction of the channel length and device dimensions of the fundamental device MOSFET. The high scaling of the CMOS technology has caused the search of alternative transistor architectures capable of overcoming the short channel effects (SCE) and the limitations of conventional inversion-mode devices. This reduction of MOSFET device has enabled remarkable increase in integrated circuit performance [1–3]. As device dimensions approaching the nanoscaled regime, the conventional MOSFET architectures are facing significant challenges, including short-channel effects, increased leakage current, threshold voltage variability, and complex fabrication requirements. To address these issues, novel transistor structures with enhanced electrostatic control have been extensively investigated.

However, aggressive scaling introduces challenges such as short-channel effects, leakage currents, mobility degradation, and manufacturing complexity [4–6]. Among emerging architectures, the Junctionless Field-Effect Transistor (JLFET) is a highly promising alternative due to its excellent scalability and streamlined manufacturing. By replacing abruptly doped source and drain junctions with a single, uniformly doped semiconductor layer, JLFETs bypass the challenges of ultra-shallow junction formation and drastically reduce device variability.

Furthermore, pairing this architecture with a double-gate structure grants exceptional gate control over the channel, which effectively mitigates short-channel effects and boosts overall performance. Junctionless transistors have emerged as promising alternatives because they eliminate abrupt source/drain junctions and use of a uniformly doped channel [7–10]. Many analytical models were developed further to use in the SPICE coding making it one of the preferred device[8, 10–14]. Many circuit based performance analysis were also studied which shows prominent

results for DG-JLFETs [15–17]. Quantum mechanical effects (QME) and analytical models under the QME were also available in the literature [18–21].

To enhance the device performance of these highly scaled transistors, it is essential to understand their underlying electrostatic behaviour. The gate capacitance and channel charge distribution govern the electrostatic behavior of field-effect transistors and significantly influence performance parameters like switching speed, intrinsic delay, and power consumption[22]. As the fundamental unit of MOS-based devices, the MOS capacitor provides a fundamental model for understanding carrier accumulation, depletion, and electric-field modulation at the semiconductor–oxide interface. Therefore, capacitance analysis is important for understanding and improving the electrostatic integrity of advanced DG JLFETs.

In this work, a TCAD-based investigation of MOS capacitor characteristics and gate capacitance behavior in a junctionless double-gate transistor is presented. The influence of channel doping and gate bias on capacitance characteristics is analyzed and compared with conventional inversion-mode devices. The results provide valuable insights into the trade-off between electrostatic control, capacitance reduction, and overall device performance in advanced junctionless transistor technologies.

1.1. Study Objectives

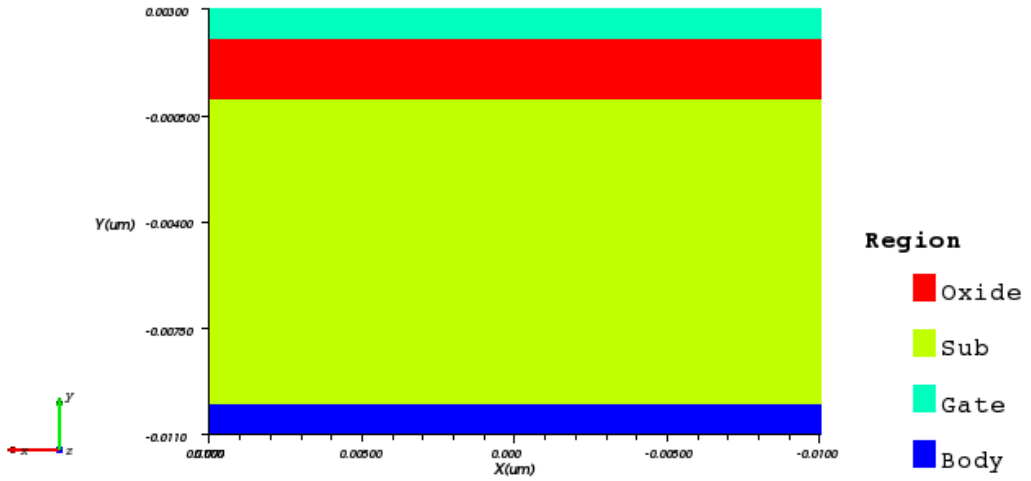
The objectives of this work are:

1) To investigate the MOS capacitor characteristics of DG-JLFETs using TCAD simulations.
2) To analyze the effect of channel doping concentration on device capacitance.
3) To study the variation of gate capacitance with gate bias voltage.
4) To examine the relationship between channel charge distribution and electrostatic behavior.
5) To evaluate the impact of capacitance characteristics on switching performance and device scalability.
6) To identify suitable design parameters for improved electrostatic control in nanoscale DG-JLFETs.

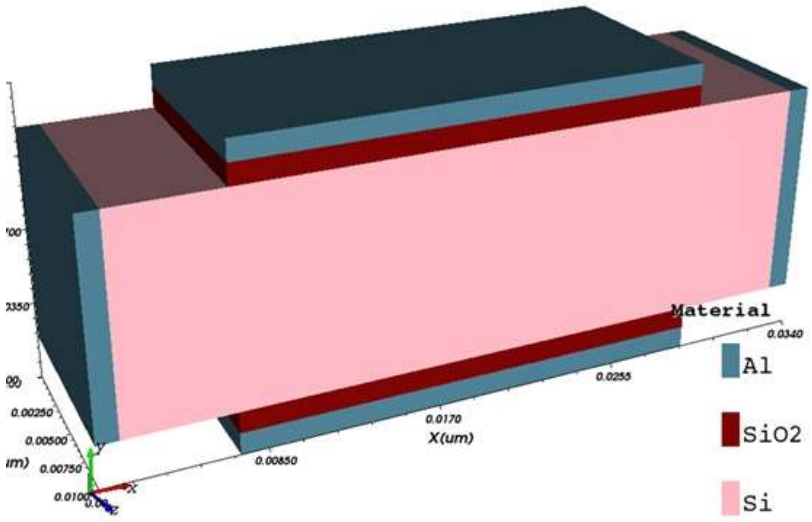
2. Device Structure and Simulation Methodology

The MOS capacitor structure used in this work was designed and simulated using the Cogenda Visual TCAD (VTCAD) software [23]. As shown in Fig. 1, the device consists of four distinct regions namely a metal gate electrode, a silicon dioxide (SiO_2) gate dielectric, a semiconductor substrate, and a bottom body contact. The gate electrode is placed above the oxide layer, forming the conventional metal–oxide–semiconductor (MOS) configuration. Fig 1(b) shows simulated diagram of the DG JLFET using Cogenda Visual TCAD (VTCAD) software. The semiconductor substrate is uniformly doped n-type silicon, while the gate oxide acts as the insulating layer that electrically isolates the gate from the body. The gate material was defined using a fixed work function, whereas the oxide layer was modelled using SiO_2 with an appropriate dielectric constant. Ohmic contacts were assigned to the gate and body terminals to facilitate capacitance extraction under varying bias conditions. The simulations were carried out using the drift–diffusion transport framework implemented in Cogenda VTCAD. Fermi–Dirac carrier statistics were employed to accurately account for carrier concentration under high doping

conditions. The resulting charge distribution and gate capacitance characteristics were extracted from the small-signal AC analysis. The capacitance–voltage (C–V) characteristics were subsequently obtained to investigate the accumulation, depletion, and inversion behavior of the MOS structure.



(a)

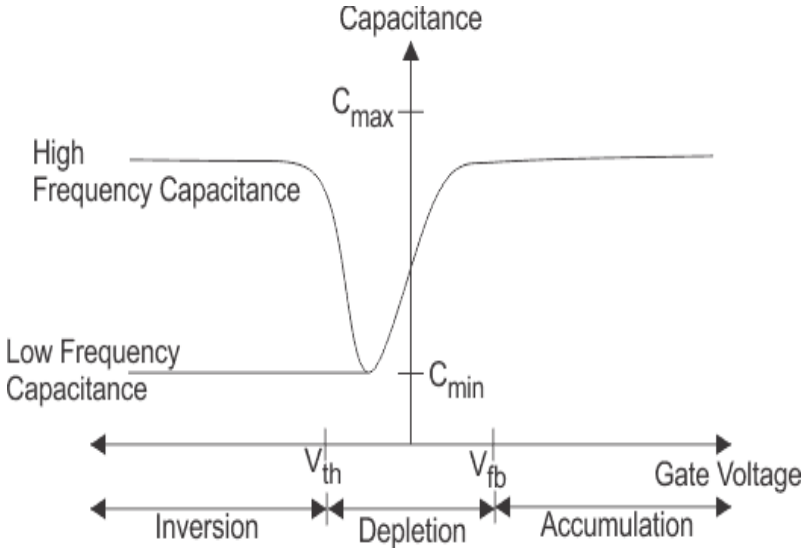


(b)

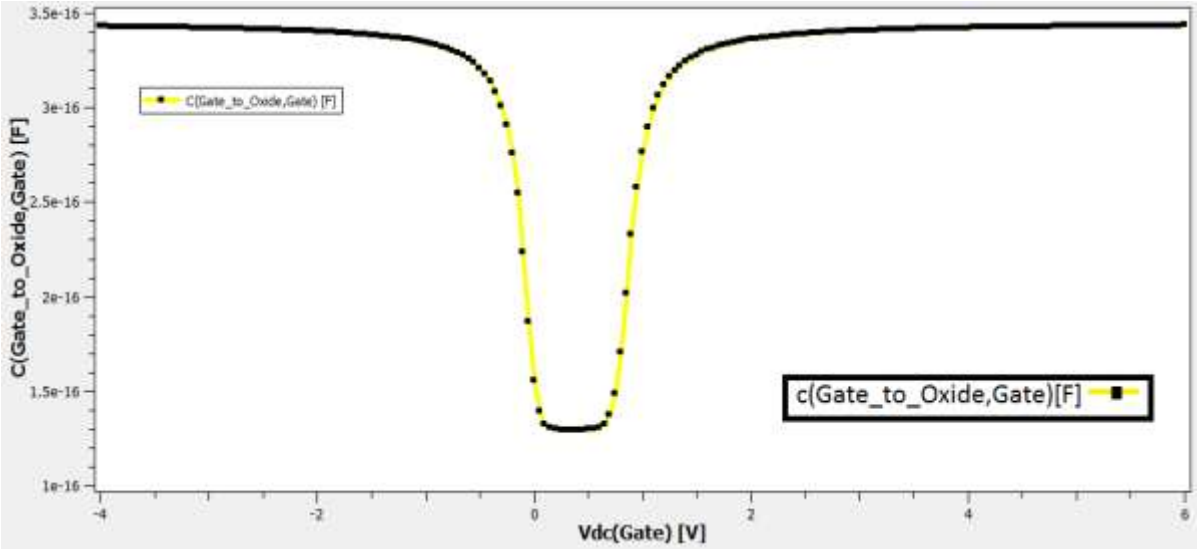
Figure 1. (a) Structural view of MOS Capacitor, and (b) Structural view of DG JLFET.

3. Results and Discussion

The typical capacitance-voltage characteristics of a MOS capacitor with n-type body are given below in Fig. 2 (a) and simulated results in Fig. 2 (b). We are able to get theoretical curve via TCAD simulations which justifies the correctness if the simulation setup. The operating mechanism of an n-channel DGJLFET differs from that of a conventional n-channel DGFET. In the subthreshold region, the heavily doped channel is fully depleted. As the gate voltage increases, the depletion region shrinks and a neutral region forms at the channel center, marking the onset of bulk conduction and the threshold voltage. Further increase in gate bias leads to the flat-band condition, where the channel becomes fully neutral and the bulk current reaches its maximum value.



(a)



(b)

Figure 2. (a) Gate capacitance-voltage characteristics of a MOS capacitor with n-type body [2], and (b) C_G vs V_{GS} characteristics of a MOS capacitor obtained using TCAD.

Beyond this point, electron accumulation occurs near the channel surfaces, resulting in surface conduction similar to that of a conventional DGFET. Since surface conduction begins at a much higher gate voltage than bulk conduction, the total current in a junctionless transistor is predominantly governed by bulk current. However, for high-performance logic applications requiring large drive current, the contribution of accumulation-mode operation cannot be ignored.

Colinge et al. [24] reported that the gate capacitance of junctionless transistors is relatively low due to the central location of the conducting channel. In this work, the gate capacitance is investigated for different channel doping concentrations and compared with those of double-gate inversion-mode and double-gate junctionless transistors under both lightly doped and heavily doped channel conditions.

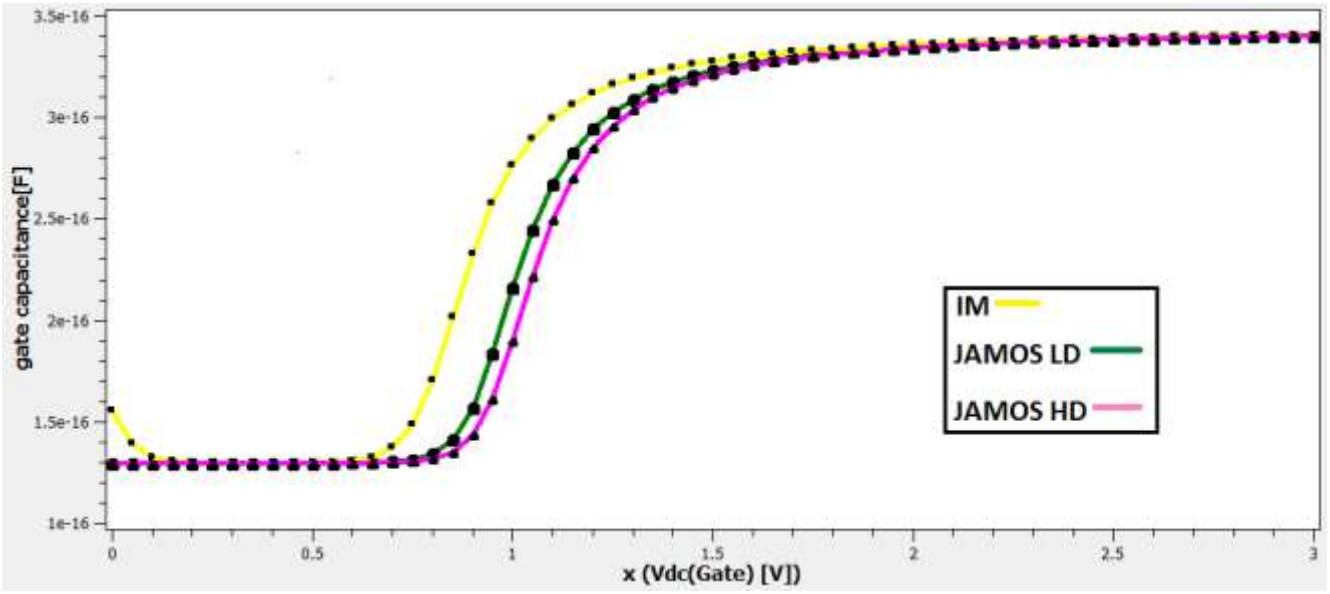


Figure 3. Measured gate capacitance vs V_{GS} at L=20 nm at V_{DS}=0.05 V.

Fig. 3, shows the gate capacitance characteristics of the IM and JAMOS devices at L=20 nm and V_{DS}=0.05V. At low gate voltages, all devices exhibit a low and nearly constant capacitance due to depletion of the channel region. As V_{GS} increases, the capacitance rises sharply as carriers accumulate in the channel. The IM device shows an earlier capacitance transition, while the JAMOS devices require a higher gate voltage because conduction develops through the channel center before surface accumulation occurs. At higher gate voltages, all curves converge to nearly the same saturation capacitance, indicating strong channel formation and similar oxide-limited behavior.

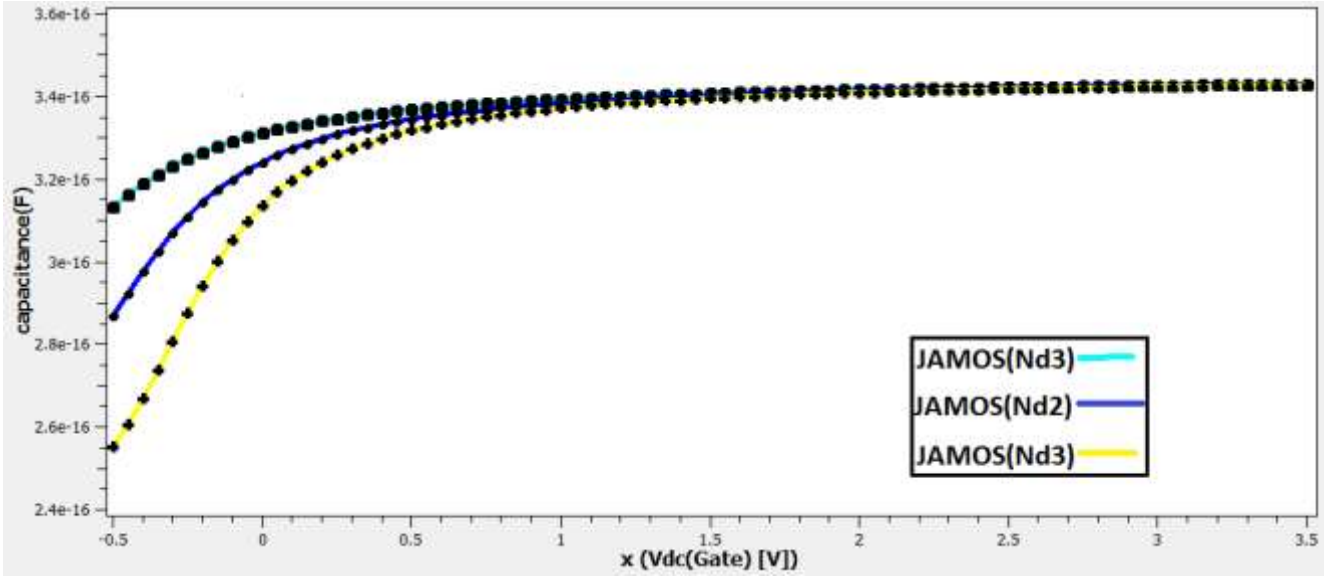


Figure 4. C_G for JAMOS with different doping concentrations.

Fig. 4, shows the gate capacitance variation of JAMOS devices for different channel doping concentrations of N_{d1}= $5\times10^{19}cm^{-3}$, N_{d2}= $2\times10^{19}cm^{-3}$, N_{d3}=$1\times10^{19}cm^{-3}$. The capacitance remains low at small gate voltages due to channel depletion and increases with V_{GS} as carriers accumulate, and eventually saturates at higher gate voltages. A higher channel doping concentration results in lower gate capacitance and a more gradual capacitance transition,

owing to the centrally located conduction path characteristic of junctionless operation. While the reduced capacitance is beneficial for lowering intrinsic switching delay, it is accompanied by a reduction in drive current. At large gate voltages, all curves converge to nearly the same saturation capacitance.

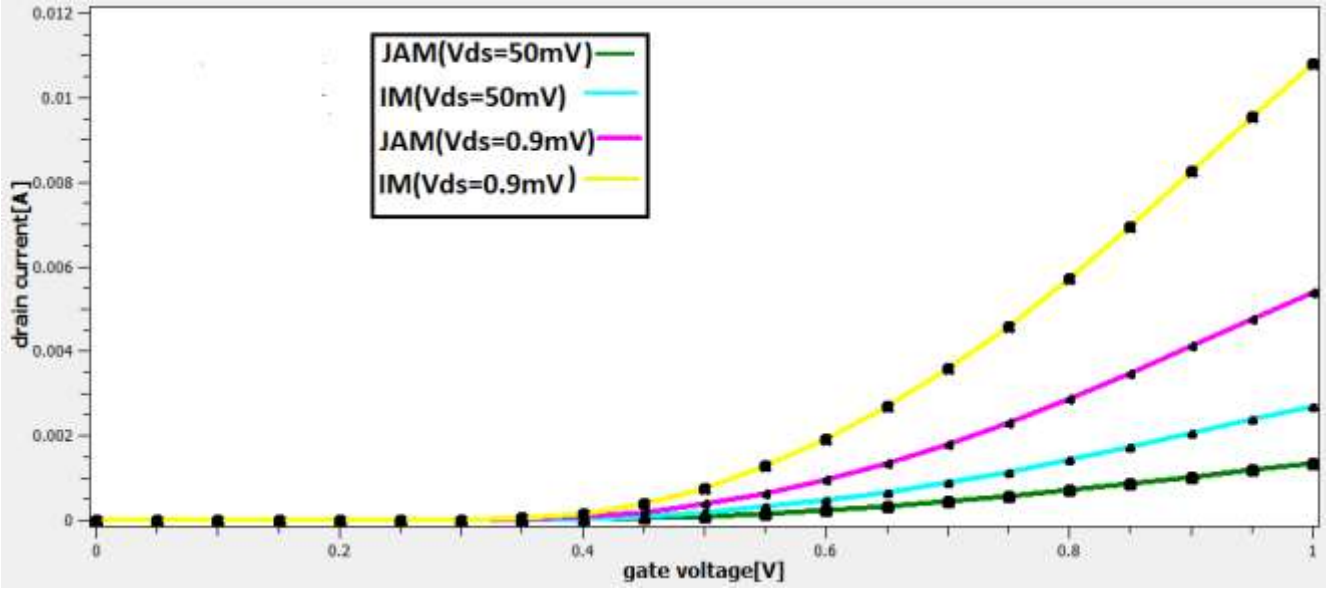


Figure 5. Output characteristic in both JAM and IM devices at V_{DS} =50 mV and 0.90V.

Fig. 5, compares the transfer characteristics of JAM and IM devices at V_{DS} =50 mV and 0.9 V. As expected, the drain current increases with gate voltage and is significantly higher at larger drain bias. The IM device consistently delivers higher drive current than the JAM device due to its stronger gate control and lower threshold voltage. In contrast, the JAM device exhibits reduced drain current, particularly at high bias, owing to its higher threshold voltage and mobility degradation caused by impurity scattering in the heavily doped channel. Although JAM benefits from lower gate capacitance, its weaker electrostatic control results in inferior current drive and scalability compared with the IM device.

The simulated MOS capacitor accurately captured the accumulation, depletion, and inversion regimes. Results show that the gate capacitance of JAM devices decreases with increasing channel doping due to the shift of the charge centroid toward the silicon body center, which increases the effective oxide thickness. Although the reduced capacitance is beneficial for lowering switching delay, higher doping also increases the threshold voltage and degrades carrier mobility through impurity scattering. Consequently, compared with inversion-mode devices, JAM transistors offer lower gate capacitance but exhibit reduced drive current and weaker gate control, particularly at higher bias conditions, highlighting the trade-off between switching speed and current drive capability.

4. Conclusion

This study investigated the impact of MOS capacitor characteristics on double-gate junctionless transistors using TCAD simulations. The results show that channel doping strongly influences gate capacitance and device performance. Higher doping reduces gate capacitance, benefiting switching speed, but also increases threshold voltage and impurity scattering, leading to lower drive current. Therefore, careful optimization of channel doping is

essential to achieve an effective trade-off between capacitance reduction and current-driving capability in advanced nanoscale junctionless devices.

4.1. Future Scope

1) Development of analytical capacitance models for DG-JLFETs suitable for circuit-level simulations.

2) Investigation of quantum mechanical effects on capacitance behavior in deeply scaled devices.

3) Evaluation of high-k gate dielectrics for improved electrostatic control and capacitance optimization.

4) Extension of the study to advanced multi-gate structures such as nanowire and gate-all-around junctionless transistors.

5) Analysis of the impact of capacitance characteristics on logic and memory circuit performance.

6) Optimization of device geometry and channel doping for enhanced scalability and performance.

Declarations

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The authors received no specific funding for this research.

Competing Interests Statement

The authors declare that they have no competing interests.

Consent for Publication

Both the authors have reviewed and approved the manuscript for publication.

Authors' Contributions

N. Bora conceived the study, developed the analytical framework, performed the investigation, analyzed the results, and prepared the manuscript; N. Deka contributed to simulation validation, manuscript review, and supervision; all authors read and approved the final manuscript.

Informed Consent

Not Applicable.

Availability of Data and Material

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

Institutional Review Board Statement

Not Applicable.

Ethical Approval

Not Applicable.

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Declaration of Artificial Intelligence

Artificial intelligence tools were used only for language editing and grammatical improvement of the manuscript; all scientific content, analysis, and conclusions were developed and verified by the authors.

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