Asian Journal of Applied Science and Technology (AJAST)
Volume 1, Issue 4, Pages 24-27, May 2017

A Digital PLL Using Digitally Controlled Oscillator for Low Power Consumption

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Article Received: 27 April 2017 *Article Accepted: 07 May 2017* *Article Published: 11 May 2017*

ABSTRACT

This paper describes a design of digital phase locked loop (DPLL) by replacing voltage controlled oscillator (VCO) by digital controlled oscillator (DCO) and to design a divide by 8 counter block. By designing the DCO and counter the power consumption is reduced in the DPLL circuit. The netlist is generated by using HSPICE tool and the power estimated from DCO is 1.0356*10^-4. The comparison between VCO and DCO is tabulated and from this tabulation the result shows that DCO consumes less power than VCO.

Keywords: Phase locked loop, Digital phase locked loop, Bang bang phase detector, DCO, VCO and Divide by N counter.

1. INTRODUCTION

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, adjusting the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is "fed back" toward the input forming a loop.

The advanced version PLL is Digital Phase Locked Loop (DPLL). The analog PLLs (APLLs) are still widely used, but digital PLLs (DPLLs) are attracting more attention for the significant advantages of digital systems over their analog counterparts. These advantages include superiority in performance, speed, reliability, and reduction in size and cost.

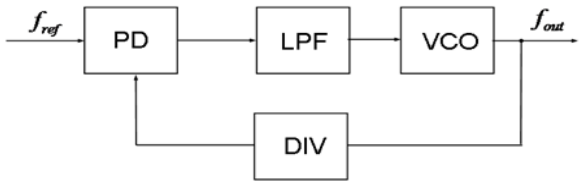

Fig.1 Basic Block Diagram of DPLL

The first component in our DPLL is the phase detector. The two types of phase detector are XOR gate and a phase frequency detector (PFD), have significantly different characteristics. The phase detector compares the phase difference between the two input signals such as data and clock. The loop filter is the brain of the DPLL. In this, we select the loop filter values in order to keep the DPLL from oscillating. If the loop-filter values are not selected correctly, it may take the loop too long to lock, or once locked, small variations in the input data may cause the loop to unlock. A Voltage controlled oscillator is an oscillator with an output signal whose output can be varied over a range, which is controlled by the input DC voltage. It is an oscillator whose output frequency is directly related to the voltage at its input. Counter is a device which works on each edge of the clock and count the number of clock pulses. Design of DCO [1] is presented which is based on SR trigger. [2] Shows that the phase locked loop is used as a multiplying circuit. Digital phase locked loop for high speed clock generation by using a digital control mechanism and ring oscillator [3].

This brief is arranged as follows. Section II describes the existing VCO architecture. The implementation of the proposed DCO using HP 45nm CMOS process is presented in Section III. Section IV shows simulation and measurement results of DCO. Section V concludes with a summary.

2. EXISTING SYSTEM

VCO:

To evaluate the amount of leakage current via the frequency, a method that converts current into frequency using a ring-type VCO was used, as shown in Fig. 7. The VCO consists of a current buffer and a three-stage ring oscillator with differential delay cells, as shown in Fig. 7(b) [4], [5]. Using a linear and wide-frequency-tunable architecture [4], this VCO is designed to provide a highly linear response for input currents between 0.5 μA and 0.5 mA (27 000 times the actual leakage current from the DUTs).

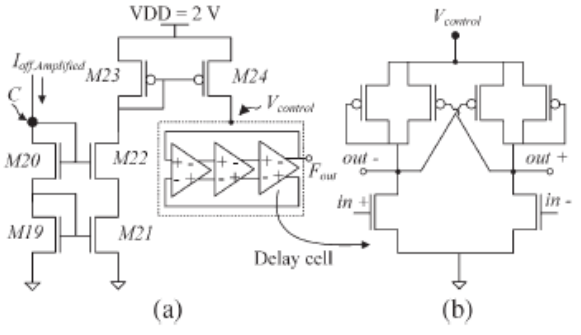

Fig.2 schematic of a) VCO b) its delay cell

Then, it converts the current to frequency values between 7 and 430 MHz. When the VCO oscillates, the second harmonic components appear at the *V* control node, which modulates the current of the *I*off, Amplified from the CA if the VCO is directly connected to the CA block. Thus, one must isolate the VCO from the CA to prevent this problem and to stabilize the leakage current of the DUT. A current buffer stage, formed by *M*19, *M*20, *M*21, and *M*22 in Fig. 7(a), is added to the VCO block for this reason.

3. PROPOSED SYSTEM

DCO:

DCO is an oscillator circuit that generates analog signal whose frequency is controlled by digital input. But, in case of VCO, frequency is set by the control voltage. The following diagram shows the basic block diagram of DCO.

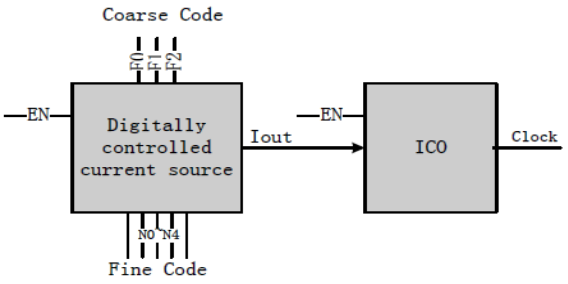

Fig.3 Basic Block Diagram of DCO

The functional block diagram of DCO circuit proposed in paper is shown in Fig. 2. It is composed of current controlled oscillator and digitally controlled current source. F0~F1 is the Coarse Code of tuning the output current from the digitally controlled current source, while N0~N4 is the Fine Code. The controlled bits F0~F1 and N0~N4 influence the value of output current so as to determine the frequency of the output clock signal from the current controlled oscillator.

a) Current controlled oscillator:

This current controlled oscillator is the core of DCO and is designed based on the logic of SR trigger and the capacitors charging time from input current. The circuit proposed is shown in Fig. 3. The oscillation is simply performed as follows:

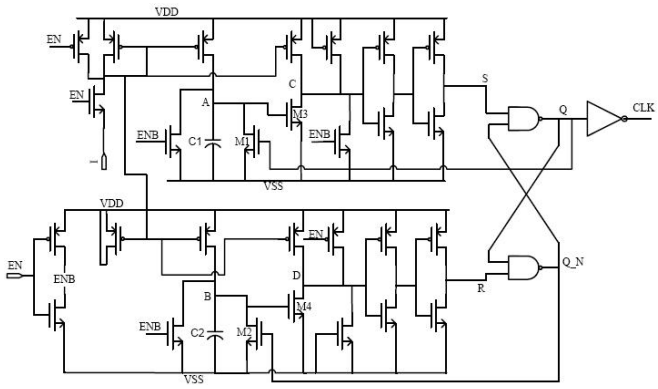

Fig.4 The current controlled oscillator circuit.

Fig. 4 illustrates the oscillator waveform signal. When EN is "low" while ENB is "high", so that V_C always maintain "low" level state while V_D is "high" all the time, these result in that V_S and V_{QN} are "low", nevertheless V_R and V_Q is "high", and the output sign CLK of oscillator is "low".

When EN is "high" and ENB is "low", V_Q is "high" initial, V_A is pulled down to "low" for the MOSFET M1 is conductive and then M3 becomes cut-off bring on that V_C start to rise up to "high" from "low" and V_S is "high". On the other hand, V_{QN} is "low" initial, the mirror current from the Digitally controlled current source charges the capacitor C2 so that the voltage V_B rises up to the threshold voltage of M4 gradually. When V_B exceeds the threshold voltage, M4 is conductive, V_D begin to drop down and V_R complete the transition from high to low. At present, V_R is "low" while V_S is high result in that is V_Q "low" while V_{QN} is "high", the oscillator complete the flip of output sign CLK.

When is V_Q "low" while V_{QN} is "high", V_B is pulled down to "low" rapidly because M2 is conductive so that V_R changed back to "high" quickly. On the other hand, M1 is cut-off so that the mirror current from the digitally controlled current source charges the capacitor C1, V_A rises up to the threshold voltage of M3 gradually. When V_A exceeds the threshold voltage, M3 is conductive, V_C begin to drop down and V_S complete the transition from high to low. At present, V_S is "low" while V_R is high result in that V_Q is "high" while V_{QN} is "low", the oscillator complete the flip of output sign CLK.

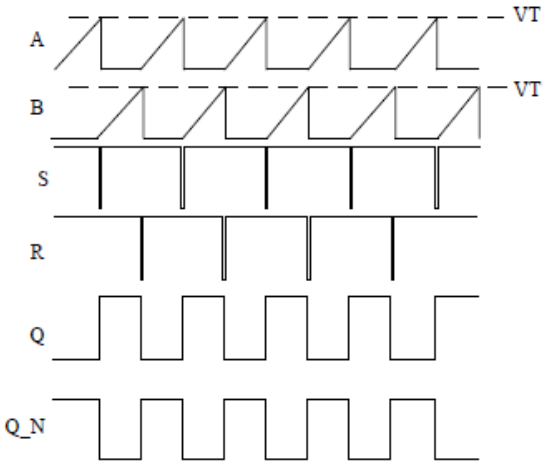

Fig.5 The oscillator circuit schematic waveform signal

So that C1 and C2 capacitors are alternately charging and discharging in the circle, and R, S change their "high" and "low" level with 180 degree phase difference by RS flip-flop.

The oscillator produces a fixed frequency clock signal CLK finally. The period of the oscillator is determined by charging time of capacitors C1 and C2. The calculation formula of the oscillation periodic time is given by:

$$T = 2\int_0^{V_T} \frac{C}{I} dv$$

Where, C is the capacitance of capacitor C1 and C2 (C1=C2), I is the input currents. So the frequency control mechanisms of DCO are based upon the control of the input currents.

b) Digitally Controlled Current Source:

It is mentioned that the frequency of DCO is determined by the input currents in last part. The digitally controlled current source is pivotal. Fig. Shows the digitally controlled current source circuit proposed in paper. It is composed of enable controlled circuit, bias current source, voltage reference with low-power consumption and current mirrors. As for EN is "low", M12 and M13 are cut-off, bias current source can't provide current to the mirror branch; When EN is "high", the circuit work effectively. The current mirrors mosfets is composed of M19~M24 and M30~M32. The size ratios of M19~M24 are increased by two times while size ratios of M30~M32 are unchanged. In the current reference circuit which uses low-voltage cascode structure provide a low voltage supply accommodation. In the circuit shown in Fig. 5, the gate of M8 and M9 is connected with the drain of M13, while the gate of M10 and M11 is connect with the output Vb of voltage reference with low-power consumption. At this low voltage cascode structure compared with ordinary cascode structure, it occupies a voltage margin is reduced from 2Vgs to Vgs, to accommodate low voltage supply conditions.

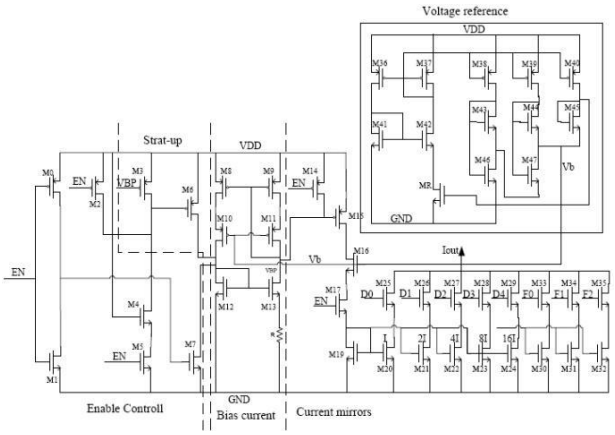

Fig.6 The digitally controlled current source circuit

In the consideration of low power consumption, it is prerequisite to design special voltage bias circuit for low voltage cascode to provide bias voltage Vb. The circuit is illustrated in Fig. 6.

The circuit consists of a current source sub-circuit and a bias-voltage sub-circuit. The current source sub-circuit is a modified β multiplier self-biasing circuit that uses a MOS resistor MR instead of ordinary resistor. The bias-voltage sub-circuit consists of a transistor (M46) and two source-coupled pairs (M43-M47 and M44-M45). The gate-source voltages of M42 and M46 in the bias voltage sub-circuit and MR in the current source sub-circuit and current mirror form a closed loop [4]. All the MOSFETS in bias-voltage sub-circuit and current source sub-circuit except for MR are operated in the sub-threshold region for nA-level current consumption.

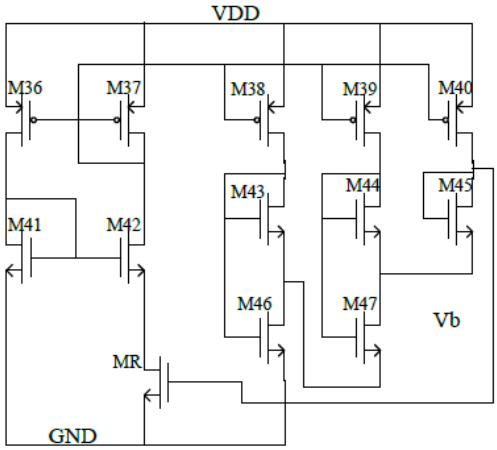

Fig.7 The voltage reference circuit with low power consumption

The subthreshold drain current of a MOSFET is an exponential function of the gate-source voltage Vgs and the drain-source Vds.

4. SIMULATION RESULTS

Table 1: Tabulation for Digitally Controlled Current Source for Different Input Codes

COARSE CODES	FINE CODES	Iout (ua)
000	00000 11111	28.7 0.337
001	00000 11111	38.5 4.02
010	00000 11111	38.7 1.42
011	00000 11111	38.2 2.11
100	00000 11111	29.9 0.396
101	00000 11111	38.5 3.57
110	00000 11111	35.2 0.554

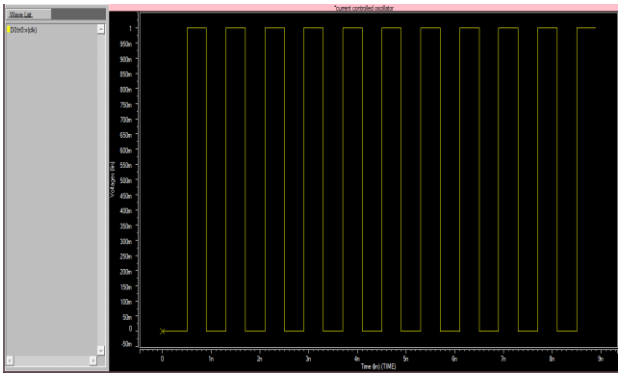

Fig.8 The transient waveform of output clock signal

5. CONCLUSION

Hence, the design of digital phase locked loop (DPLL) by replacing voltage controlled oscillator (VCO) by digital controlled oscillator (DCO) and to design a divide by 8 counter block has done. By designing the DCO and counter the power consumption is reduced in the DPLL circuit. The netlist is generated by using HSPICE tool and the power estimated from DCO is 1.0356*10^-4. The comparison between VCO and DCO is tabulated and from the tabulation the result shows that DCO consumes less power than VCO.

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