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Reconfigurable OFDM Transmitter for LTE Standard

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ABSTRACT

OFDM is a multi-carrier modulation technique with densely spaced sub-carriers that has gained a lot of popularity among the broadband community in the last few years. Orthogonal frequency division multiplexing (OFDM) is an established technique for wireless communication applications. The proposed OFDM transmitter which can capable of generating multiple FFT/IFFT frames without any hardware modifications. For making OFDM transmitter with a reconfigurable property, a novel frame rate controller with enhanced memory limit is constructed. The generated IFFT values are stored in memory block and then with the help of frame rate controller the OFDM blocks converted into 32, 64, and 128 with respect to required applications. The proposed model implemented and verified in Xilinx 14.1 ISE. The result showing that proposed OFDM capable of generating multiple bits for 5G applications.

Keywords: OFDMA, FFT, IFFT, Reconfiguration, IDE and Multicarrier.

1. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) is a digital multi-carrier modulation scheme that extends the concepts of single subcarrier modulation by using multiple subcarriers within the same single channel. Rather than transmit a high-rate stream of data with a single subcarrier, OFDM makes use of a large number of closely spaced orthogonal subcarriers that are transmitted in parallel. Each subcarrier is modulated with a conventional digital modulation scheme (such as BPSK, QPSK, etc.) at low symbol rate. However, the combination of many subcarriers enables data rates similar to conventional single-carrier modulation schemes within equivalent bandwidths.

In special, Orthogonal Frequency Division Multiplexing (OFDM) is considered the science for the next-generation broadband wireless techniques [1]. In point of fact, it has been adopted for a lot of requisites, comparable to 3rd generation Partnership challenge-long run Evolution (3GPP-LTE), Digital Audio Broadcasting (DAB), Digital Video Broadcasting–Terrestrial (DVB-T), Digital Video Broadcasting-Handheld (DVB-H), and IEEE 802.11 [2].

Nonetheless, OFDM methods requires intensive computing algorithms, so it's imperative to put into effect them making use of state-of-the-art high performance instruments. Field Programmable Gate Array (FPGA) is a very cost effective and enormously bendy resolution, which permits quick prototyping, and re-usability of functional modules and likewise presents system efficiency sophisticated to normal options centered on Digital sign Processors (DSP). Additionally, FPGA designs can also be comfortably migrated to Application-Specific Integrated Circuits (ASICs).

In [3] a configurable transmitter structure for specific and implicit Training (IT) communications systems is proposed. This transmitter helps 4/16/64-QAM (Quadrature Amplitude Modulation) modulation in superimposed training (ST) and data-dependent superimposed training (DDST). However, the data rate is constant, and the transmitter did not do not forget a pulse-shaping filter.

In [4] a Multi-standard Transmitter is presented. Its structure incorporates each implicit and explicit training modes into a reconfigurable transmitter for application defined Radio (SDR) functions. It additionally considers a pulse-shaping filter and is capable to participate in a few modulation schemes, akin to: four/sixteen/64 QAM, Binary section Shift Keying (BPSK), Offset phase Shift Keying (OQPSK), Differential Binary phase Shift Keying (DBPSK), and Differential segment Shift Keying (DQPSK). However, both, [3] and [4] are only for single carrier systems.

A reconfigurable architecture for an OFDM modulator is described in [5]. Such transmitter was once proven for Chinese language cell Multimedia Broadcasting (CMMB) and DAB techniques, but not for LTE purposes. Furthermore, a mental Property (IP) core was used for the Inverse fast Fourier become (IFFT) processing.

In [6], a modulator for IEEE 802.11a is mentioned. Its engine is founded on a constant-size 64-point Xilinx IP core, suitable for IEEE 802.11a. Hence, it is not able to supporting different standards. In contrast to previous works, a fast OFDM transmitter presented in this paper. Neither IP cores nor pre-designed components have been used in an effort to assurance portability. Our study case was once the 3GPP-LTE standard for downlink frames, that is, Orthogonal Frequency Division multiple access (OFDMA). Nevertheless, it is reconfigurable accomplish to support OFDM functions.

The remaining portion of this paper is organized as follows: section 2 briefly explains about the design and implementation of proposed OFDM transmitter, section 3 contains simulation results, section 4 gives conclusion about this research paper and section 5 contains related works.

2. DESIGN AND IMPLEMENTATIONS OF THE PROPOSED OFDM TRANSMITTER

The proposed OFDM transmitter is shown in Fig.1. It is composed of following modules: Serial Data Source (SDC), Encoder, Serial to Parallel (STP), FFT/IFFT processor, Parallel to Serial Convertor (PTS), Cyclic Prefix (CP), Frame Rate Controller (FRC), and Transmission Channel (TC). All blocks are operating together as explained below.

Bank Register (BR) consists of three types of information such as data configuration, pilots, and data (both user and control data). These three types of information are store in BR. The input data of proposed OFDM transmitter is obtained from the SDS. Then this serial input data is given to the encoder. This encoder module consists of correlator and BPSK modulator. In this encoder section the signal is modulated by using BPSK modulator. After this modulated signal is given to the STP. This STP module perform serial to parallel conversion process. This converted parallel data is given to the IFFT processor .The input data can converted from parallel to serial starts during the last stage of the IFFT processing. This parallel data is given to the CP. This CP adds some reference bits to the input data for an error detection purpose. In this proposed system cyclic prefix is connected with FRC. After that Frame Rate Controller manages the transmission rate of the OFDM frames required for each bandwidth (BW) specified in LTE standard.

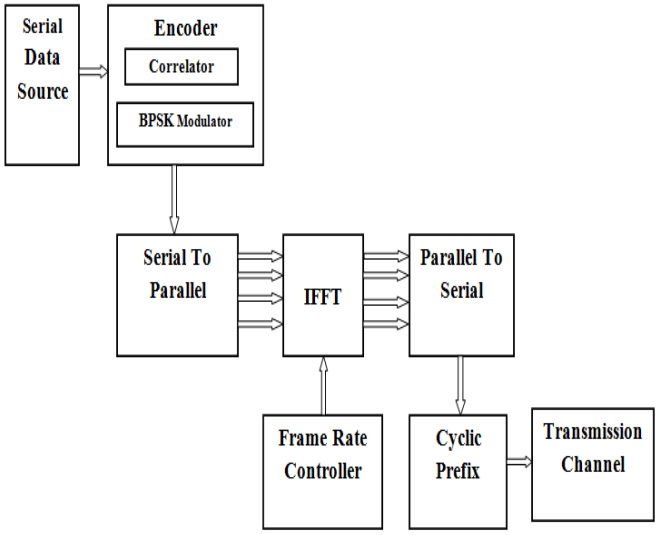

Fig.1. Block Diagram of the Proposed Reconfigurable OFDM Transmitter

Finally, this input data is given to the transmission channel (TC).The entire process is repeated to generate the rest of the OFDM symbols which comprise the frame. An explanation of the main modules of the OFDM transmitter is detailed below.

Binary Phase-shift keying (BPSK) is a digital modulation scheme that conveys data by changing, or modulating, two different phases of a reference signal (the carrier wave). The constellation points chosen are usually positioned with uniform angular spacing around a circle. Phase-shift keying (PSK) is a digital modulation scheme that conveys data by changing (modulating) the phase of a reference signal (the carrier wave). The modulation is impressed by varying the sine and cosine inputs at a precise time. It is widely used for wireless LANs, RFID and Bluetooth communication. It is considered to be more among all the modulation types due to difference of 180 degree between two constellation points. Hence it can withstand severe amount of channel conditions or channel fading. It is used in OFDM and OFDMA to modulate the pilot subcarriers used for channel estimation and equalization. As we know different channels are used for specific data transmission in cellular systems. The channels used to transmit system related information which are very essential are modulated using BPSK modulation.

2.1 Serial-To-Parallel Conversion

Conversion of a stream of data elements received in time sequence, *i.e.*, one at a time, into a data stream consisting of multiple data elements transmitted simultaneously.

2.2 IFFT processor

A multi-core Variable Length (VL) FFT/IFFT processor based on Decimation-in-Time (DIT) Fast Fourier Transform (FFT) radix-2 algorithm is proposed for OFDM-engine. The N-point Discrete Fourier Transform (DFT) of an input sequence x(n) is defined as follows:

$$X(k) = \sum_{n=0}^{N-1} x(n)\, W_N^{nk}, \quad k=0, 1\ldots N-1 \qquad (1)$$

Where WN = e−j 2π N are the twiddle factors, n is the discrete time-domain index, and k is the normalized frequency-domain index. N-1the Inverse Discrete Fourier Transform (IDFT) can be expressed as:

$$X(n) = \frac{1}{N} \sum_{K=0}^{N-1} X(k) W_N^{-nk}, \quad n=0, 1\ldots N-1 \qquad (2)$$

From the point of view of decimation, there are two basic types of FFT algorithms: decimation in time (DIT) and decimation in frequency (DIF). There is no difference in computational complexity between them and the number of samples must be a power of two. The DIT radix-2 FFT algorithm divides the original sequence into two N/2-point data sequences f1 (n) and f2 (n), corresponding to the even indexed and odd-indexed points of x (n), respectively. Then N-point DFT can be computed as:

$$X(k) = F_{1(K)} + W_N^k F_2(k)$$

$$X(k+N/2) = F_{1(K)} - W_N^k F_2(k) \qquad (3)$$

Where, k = 0, 1... N/2 − 1, F1 (k) and F2(k) are the N/2- point DFT of f1(n) and f2(n), respectively. The subsequences F1 (k) and F2 (k) are recursively solved applying the above formula. Thus, the elementary operation is obtained, known as DIT butterfly (BF).

2.3 Frame Rate Controller

This converts the data bit-stream (user and control data) to a sequence of modulated data, which is accepted by IFFT processor. Its internal modules are described below

Bank Register: This was designed to configure different transmitter operation modes. All of its internal registers are presented below.

• ***Data FIFO***. This is used to store data, whether user or control, which are introduced through word input. The first introduced word represents data set 1; the second introduced word represents data set 2, and so on. The first data of each set is located in the Most Significant Bits (MSB). The amount of data in each set is determined by DM (Data modulation scheme) input and Data FIFO word length.

• ***Pilot Register***. This is similar to Data FIFO. The difference is that the amount of pilots in each set is determined by Pilot Register word length divided by 2.

• ***N null Carriers and CP size registers.*** Both registers have as many locations as available bandwidths for the transmitter. The first word introduced is the parameter for the bandwidth 1, the second word introduced is the parameter for the bandwidth 2, and so on.

• ***Slot configuration register***. This has as many locations as the amount of OFDM symbols per slot. The information introduced through word input is a set used to configure each OFDM symbol. The set is defined as: {pilot distance, pilot offset, ena pilots}. The first parameter determines how many sub-carriers separate a pair of pilots in the OFDM symbol. The second determines the initial sub-carrier, where pilots are included. Finally, ena pilots parameter indicates the presence of pilots in the OFDM symbol.

• ***Frame Configuration Register***. This is employed in order to configure frame size. It has two locations; the first is used to configure the number of slot in the frame and the second for the number of OFDM symbols per slot.

2.4 Parallel-to-serial conversion

Conversion of a stream of multiple data elements, received simultaneously, into a stream of data elements transmitted in time sequence, i.e., one at a time. An 802.11a **OFDM** carrier signal (burst type) is the sum of one or more **OFDM** symbols each comprised of 52 orthogonal **subcarriers**, with baseband data on each **subcarrier** being independently modulated using quadrature amplitude modulation (available formats: BPSK, QPSK, 16-QAM, or 64-QAM).

3 SIMULATION RESULTS

Fig.2. Output Waveform of Frame Rate Controller

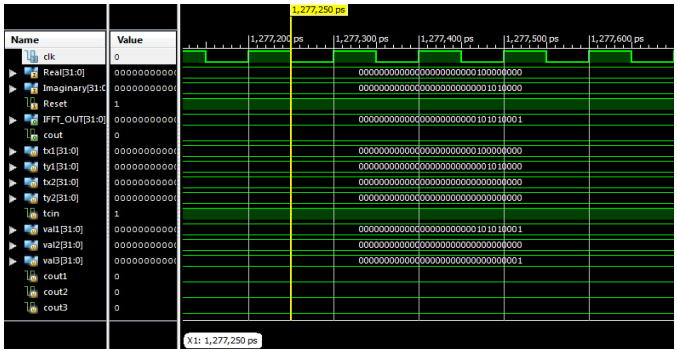

Fig.3.Reconfigurable Output Waveform of IFFT 32x

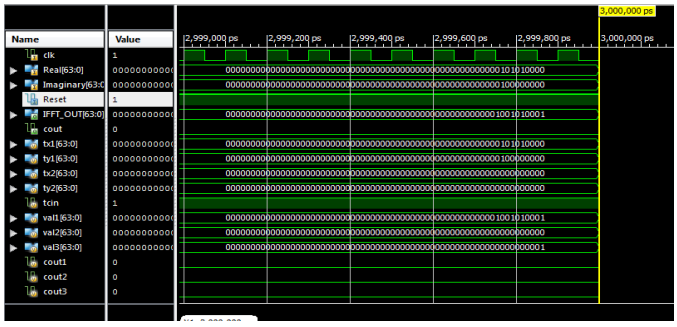

Fig.4. Reconfigurable Output Waveform of IFFT 64x

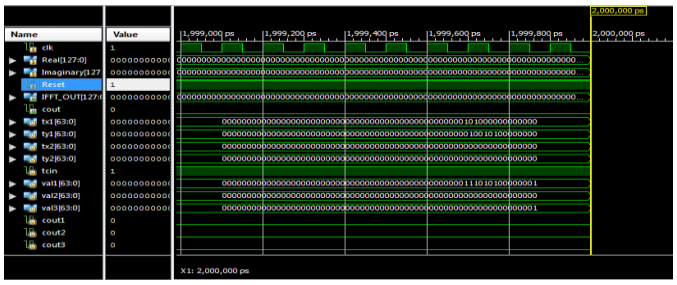

Fig.5. Reconfigurable Output Waveform of IFFT 128x

These are the simulation results which demonstrate the performance of reconfigurable OFDM transmitter in terms of frame rate controller, reconfigurable IFFT results.

Table I: Synthesis comparison of the proposed OFDM Tx

	(13)	(3)	PROPOSED
Standard	802.11a	CMMB/DAB	LTE
IFFT lengths	64	512	32,34,128
Slice Registers	2353	_	533
Slice LUTs	2814	_	252
Frequency	80MHZ	_	1 GHZ

4. CONCLUSION

In this paper, a reconfigurable OFDM transmitter for 4G-LTE applications was presented. It has the capability of selecting on-the-fly from transmission modes: 1 GHz; modulation: BPSK, frame size such as 32, 64, 128 OFDM symbols/slot, and the assembly configuration parameters of each OFDM symbol, such as the number of null carriers, the CP size, the pilot inclusion, etc. In this proposed system, a reconfigurable

IFFT/FFT was presented. To make this proposed model applicable to a fast future communication system with different system settings for its deployment with different modulation schemes in future work.

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