Asian Journal of Applied Science and Technology (AJAST)
Volume 1, Issue 5, Pages 127-130, June 2017

Hardware Implementation for the 32X32 IDCT of High-Efficiency Video Coding

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Article Received: 18 May 2017 *Article Accepted: 04 June 2017* *Article Published: 07 June 2017*

ABSTRACT

The hardware implementation of inverse discrete cosine transforms defined in High-Efficiency Video Coding (HEVC) with lower hardware complexity. The design was implemented based on separability property, which reduces the hardware complexity. The architecture was designed to reach high throughput with low latency. The total design was described in combinational, which helpful to reduce the latency. The internal multiplications of design are achieved through shift and additions, which leads to less hardware complexity. The architecture was designed using Verilog HDL and synthesized using Cadence RTL Compiler with 90nm Technology. The architecture was able to process more than 30 QFHD (3840x2160) frames per second with the delay of 40 clock cycles. The hardware can operate at a frequency of 370MHZ with a gate count of 2.5k. The architecture was designed to process 32 samples in a single clock cycle. Multiplications are done using shift and additions, which reduces the hardware complexity. The lower hardware complexity achieved through coefficients sharing, shift, and additions.

Keywords: HEVC, IDCT, QFHD, Latency and Video coding.

1. INTRODUCTION

These days, resolution and the quality of digital videos have been enhanced in a quick and consistent way. So, video encoding methods have been broadly concentrated on and created because of the expanding request in this field. These applications usually require high quality, and at the same time, the good compression rate is required. The High-Efficiency Video Coding (HEVC) standard is the latest joint video venture of the ITU-T video coding expert group (VCEG) and ISO/IEC moving picture expert group (MPEG) standard organizations, cooperating in an organization known as the joint collaborative group on video coding (JCT-VC) [1]. The objective of the JCT-VC was to increase the compression ratio by 50% and to maintain the same computational complexity. The main motivation behind the transformation technique is to concentrate the energy of image block in few couple of numerical coefficients. Inverse transforms are utilized as a part of both encoder and decoder [2]. Compression efficiency increases as the size of transform increases, at the same time increase in transform size, increases the encoder complexity [3].

Sha shen [4] proposed architecture, which uses memory for the transpose of coefficients instead of registers. Moreover, also multiple constant methods (MCM) are used to build the four/ 8 point IDCT. The regular multipliers are used to define 16/32 point IDCT. Ricardo Jeske [5] defined an architecture for 16 point inverse transform. This architecture was targeted to low cost and high throughput with a latency of 40 clock cycles. Latency was the number of cycles consumed to get first output. The proposed architecture uses coefficient reordering, factoring, and sub-expression sharing to get a high throughput of 32 samples at the cost of low hardware complexity. Finally, using multiplier less approach, the architecture was implemented to have low hardware cost. All multiplication operation employed in the 32 point IDCT design was converted into shifts and additions.

2. INVERSE DISCRETE COSINE TRANSFORM

A generic IDCT is described in equation (1), where M and N are IDCT point number, F(u, v) is the input of the position (u, v) of the input matrix, F(x, y) is the output coefficient. As seen in equation (1), without any optimization we would require a huge number of additions, multiplications which in turns consume more hardware regarding the area.

$$F(x,y) = \sqrt{\frac{2}{N}}\sqrt{\frac{2}{M}}\sum_{u=0}^{N-1}\sum_{v=0}^{M-1} Cu\, Cv\, F(u,v)\cos\left(\frac{(2x+1)u\pi}{2N}\right)\cos\left(\frac{(2y+1)v\pi}{2M}\right)$$

The essential unity of HEV is known as Transform unit (TU). It could be square in size like 4x4, 8x8, 16x16 and 32x32 samples [6]. The 1-D IDCT HEVC transform has a useful feature: the 4 point 1-D IDCT of HEVC transform is the part of 8 point 1-D IDCT which is a part of the 16 point 1-D IDCT transform, and it is repeated to implement 32 point IDCT[7,8,9, 10,11,12].

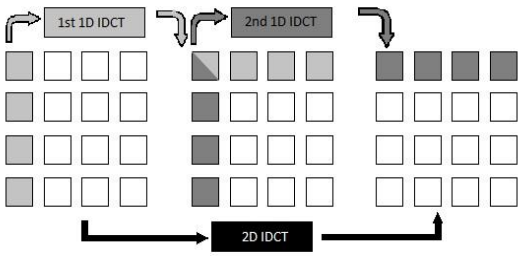

Figure 1: Demonstration of separability property

The traditional HEVC uses 1-D IDCT to generate 2-D IDCT transform with separability property to reduce the number of necessary calculations was shown in Figure.1. This property considers the 1D DCT/IDCT calculations to generate 2D DCT/IDCT with lesser number of calculations. As a first step the entire column of input matrix samples are processed through 1D IDCT, and the output coefficients are stored row

by row in transpose matrix. Then, 1D IDCT is performed again column wise for the output coefficients which are stored in the transpose matrix.

3. PROPOSED 32X32 IDCT ARCHITECTURE

The proposed architecture includes five modules: two register sets (input register and output register), two 1D IDCT architecture and one transpose matrix. Figure 2 shows the top-level architecture. This architecture was completely described using Verilog HDL and synthesized using Cadence RTL Compiler. The first block 1D IDCT takes up 32 samples per cycle from the input register. Moreover, the transpose matrix stores the output coefficients of 1D IDCT block on respective of row wise. After 32 sets of 32 samples are made ready by the input registers, the second 1D IDCT can start the process on transpose matrix by separability method. That means the first set of 32 output samples are expected in the 64th clock cycle, and a new set of 32 samples are executed in every clock cycle.

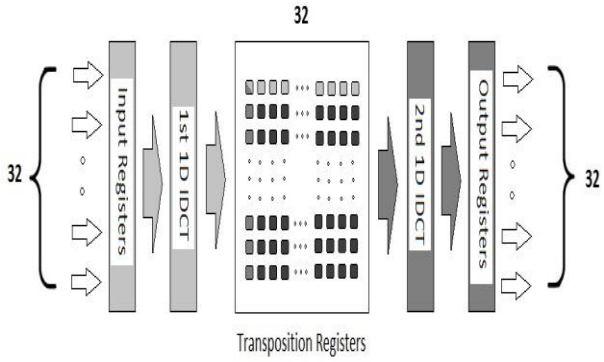

Figure 2: Top Level Architecture

The important part of 2D IDCT architecture was 1D IDCT block since two instances of 1D IDCT are utilized to generate 2D IDCT with separability property. The first part of 1D IDCT designed with specific equations, which requires multiplications. However, multipliers are costly regarding hardware and power consuming. The designed architecture uses specific multiplications used in first part of 1D IDCT block, which is shown in Table 1. 'X' represents respective input sample multiplied by respective constant.

Table 1: Example of Constant multiplications and their respective shifts and additions

Constant	Shifts and additions
86	X<<6+X<<4+X<<3+X
75	X<<6+X<<3+X<<1+X
50	X<<5+X<<4+X<<1
18	X<<4+X<<1
83	X<<6+X<<4+X<<1+X
36	X<<5+X<<2
64	X<<6

Table 2 shows the example of equations with multiplications and additions done among the input samples to get the corresponding results.

Table 2: Example of multiplication stages

Results	Operations
O_{15}	$4I_1$-$13I_3$+$22I_5$-$31I_7$+$38I_9$-$36I_{11}$+ $54I_{13}$-$61I_{15}$+$67I_{17}$-$73I_{19}$+$78I_{21}$-$82I_{23}$+$85I_{25}$-$88I_{27}$+$90I_{29}$-$90I_{31}$
EO_7	$9I_2$-$25I_6$+$43I_{10}$-$57I_{14}$+$70I_{18}$-$80I_{22}$+$87I_{26}$-$90I_{30}$
EEO_3	$18I_4$-$50I_{12}$+$75I_{20}$-$89I_{28}$
$EEEO_1$	$36I_8$-$83I_{24}$
$EEEE_1$	$64I_0$-$64I_{16}$

The results shown in Table.2 are fed to the second stage of 1D IDCT. The first 1D IDCT generate fifteen "O" outputs, seven "EO" outputs, three "EEO" outputs, one "EEEO" output and one "EEEE" output. The second 1D IDCT architecture uses Butterfly calculation. It can be done only by additions and subtractions, which was shown in Figure.3. Each black circle presents adder, and white circle presents subtractor. The square blocks are used for better understanding of stage by stage.

Butterfly Block

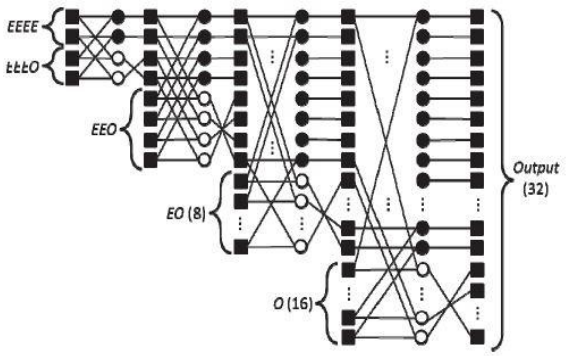

Figure 3: Butterfly Block

The final stage performs the rounding operation, as shown in Figure.4. The difference between first and second 1D IDCT are, the first 1D IDCT uses 16 bits to represent an input sample and rounding and 14 bit to represent the output sample. The second stage uses 14 bits to represent an input sample and 9 bits to represent output sample.

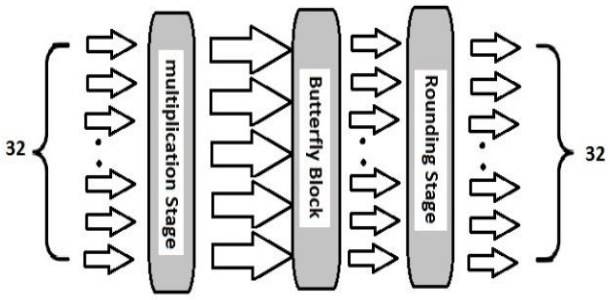

Figure 4: 1-D Inverse DCT Block Diagram

The Transpose Matrix Architecture

Figure.5 shows the transpose matrix built with registers and multiplexers. The control signal has to change at every 32 clock cycles, to modify the multiplexers select lines. That is

the data read and write operations are switched from row to column and vice versa.

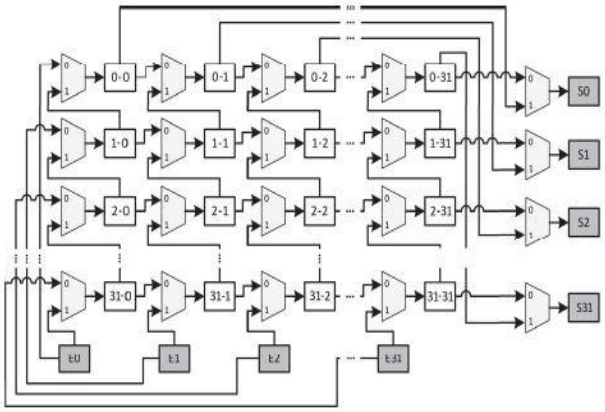

Figure 5: Transpose Matrix Block Diagram

4. RESULTS AND DISCUSSIONS

The architecture for 32X32 IDCT of High-Efficiency Video Coding is described in verilog HDL and functional verification is done using ncsim from Cadence. Logic Synthesis is done using Cadence RTL Compiler with 180nm CMOS Technology. Table.3 presents the power, area, and some gates consumed by the implementation. Table.4 presents the power consumed by the individual design modules and Table.5 presents the comparison of results with previous work. The design was able to operate at the frequency of 370MHz.

Table 3: Synthesis Results with TSMC 180nm CMOS Technology

	Parameter	value
1	Power	15848(µw)
2	Gate count	2589
3	Area	24927

Table 4: Power consumption

	Module name	Power(µw)
1	IDCT	4011.788
2	Transpose Matrix	10194.626
3	Butterfly block	2337.386
4	Multiplications	384.819

Table 5: Comparison of results

	Parameter	This work	Shen [7]
1	Transform type	2D IDCT	2D IDCT
2	Transform size	32	4/8/16/32
3	Technology	90nm	130nm
4	Multipliers	No	Yes
5	Samples per Cycle	32	4
6	Frequency	370	350
7	Latency	40	261

5. CONCLUSION

In this work, the hardware implementation for the 32X32 IDCT is done. The main goal of this work is to achieve high throughput and to utilize lesser hardware resource. The high throughput is achieved through parallelism, which was able to process 32 input samples per clock cycle. The lesser hardware complexity is achieved through coefficients sharing and multiplier-less approach. Synthesis results are targeted to Cadence RTL Compiler with 90nm technology. Thus the register based transpose matrix consumes more power, and hence there is a need for optimization in transpose matrix.

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