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Energy Efficient Full Adders for Arithmetic Applications Based on GDI Logic

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ABSTRACT

Addition is a fundamental arithmetic operation and acts as a building block for synthesizing of all other operations. A high-performance adder is one of the key components in the design of Application Specific Integrated Circuits (ASIC). In this work, three low power full adders are designed with full swing AND, OR and XOR gates to reduce threshold voltage problem which is commonly encountered in Gate Diffusion Input (GDI) logic. This problem usually does not allow the full adder circuits to operate without additional inverters. However, the three full adders are successfully realized using full swing gates with the significant improvement in their performance. The performance of the proposed design is simulated through SPICE simulations using 45 nm technology models.

Keywords: GDI Logic, Full adder and Full swing.

1. INTRODUCTION

Adders are extensively used circuit elements in Very Large Scale Integration (VLSI) systems such as Digital Signal Processing (DSP) processors, microprocessors etc. It is the nucleus of many other operations like subtraction, multiplication, division and parity checkers and addresses calculation. In most of the digital systems, adders lie in a critical path which influences the overall system performance. Hence, enhancing adder's performance is becoming an important goal. The reason behind is that the battery technology does not advance at the same rate as the microelectronics technology. There is only a limited amount of power available for the mobile systems. Therefore, low power design has become a major design consideration.

The advances in VLSI technology allow hardware realization of most computing intensive applications such as multimedia processing, DSP, to enhance the speed of operation. Moreover, with increasing demand, the researchers are driven to strive for smaller silicon area, higher speed, longer battery life and enhanced reliability. The importance of digital computing lies in full adder design. The design criteria for full adder are usually multifold. Transistor count, which is one of the attributes, determines the system complexity of arithmetic circuits like multiplier, Arithmetic Logic Unit (ALU), etc. Power consumption and speed would be the other two important criteria when it comes to the design of full adders. However, they have a contradictory relationship with each other.

Therefore, power delay product or energy consumption per operation has been introduced to accomplish optimal design tradeoffs. The performance of digital circuits can be optimized by proper selection of logic styles. Gate Diffusion Input (GDI) is a lowest power design technique which offers improved logic swing and less static power dissipation. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors. In this paper, an efficient methodology for digital circuit such as AND, OR, and XOR gates with full swing is implemented. After that, three full adders are proposed based on the full swing gates in a standard 45 nm technology.

2. GDI LOGIC

The basic GDI cell is shown in below Fig.1. GDI logic cell consists of four terminals. They are:

1) G (Common Gate input of NMOS and PMOS transistor)
2) P (Outer diffusion node of PMOS transistor)
3) N (Outer diffusion node of NMOS transistor)
4) Out (Common diffusion node of both transistors)

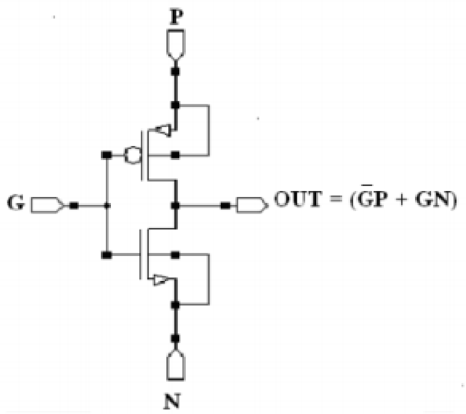

Fig.1. GDI basic cell

Table I, shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. In this paper, most of the designed circuits were based on theF1 and F2 functions. The reasons for this are as follows: 1) Both F1 and F2 are complete logic families. 2) F1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any NMOS is constantly and equally biased. 3) When N input is driven at high logic level and P input is at low logic level, the diodes between NMOS and PMOS bulks to Out are directly polarized and there is a short between N and P, resulting in static power dissipation.

Table I. Various logic functions of GDI cell for different input configurations

N	P	G	Out	Function
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

3. PROPOSED FULL ADDERS IN GDI

In this section, three proposed full adder designs featuring GDI with full swing logic are discussed with the goal to minimize the circuit complexity and to achieve speed at cascaded operation. The strategy is to avoid threshold voltage losses with the help of full swing gates.

3.1. Basic gates for full adder design

The logic function of full adder can be represented as,

$$\text{Sum}= A \text{ XOR } B \text{ XOR } C_{in} \quad (1)$$

$$C_{out}= A \text{ AND } B + B \text{ AND } C_{in}+ A \text{ AND } C_{in} \quad (2)$$

From Eqs. (1) and (2) three basic gates are needed for implementing the function.

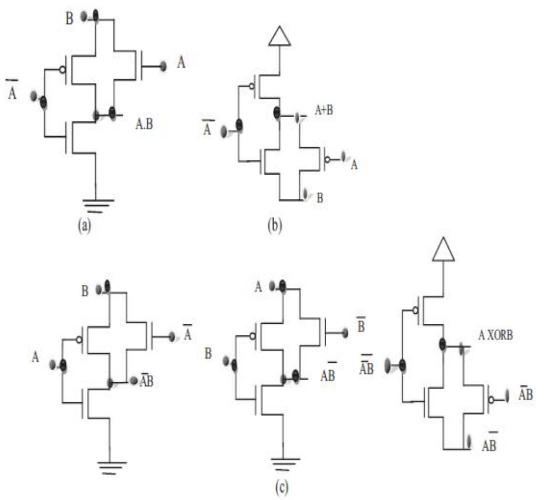

Fig.2. Full swing gates based on F1 and F2 (a) AND (b) OR and (c) XOR

3.2. Full swing AND, OR and XOR gates using F1 and F2 functions

Conventionally universal gates, namely NAND and NOR can be used to realize any logical expression. Similarly, in GDI, two functions are available, namely, F1 (AB) and F2 (A + B) to realize logical expression. These two functions are also suffering from a threshold voltage drop. Swing restoration transistor provided at the output to take care of threshold voltage loss and the schematic of AND, OR and XOR gates using F1 and F2 functions are shown in Fig 2. It increases the transistor count from 2 to 3 for the design of AND and OR yet the full swing operation can be achieved.

The choice of F1 and F2 for AND and OR gates will be good since a less number of transistors also provides full swing like CMOS. However, F1 and F2 based XOR gate implementation lacks CMOS based design. The reason might be one of the following:

(i) XOR gate based on F1 and F2 needs a total of 9 transistors, which is twice that of the transistors required for GDI logic. Therefore, it cuts off the goal of GDI logic, i.e. function realization using minimal transistor.

(ii) Due to increased transistor count, the overall input gate capacitance (Cg) of the XOR function increased since Cg is a direct function of the number of transistor seen by the inputs.

(iii) The intermediate nodes can be increased slightly; this might lead to a number of glitches which are the sources of power consumption.

The realization of AND and OR gates with full swing can be possible using F1 and F2 functions, respectively, and operate relatively better than conventional design though not suitable for XOR realization.

But XOR-XNOR circuits are basic building blocks in various arithmetic circuits such as adders, multipliers, compressors, comparators, etc. They provide an intermediate output to generate the final sum and carry the full adder.

Also the importance of XOR-XNOR functions, implementations like an adder and multiplier. Therefore, full swing XOR is necessary to drive successive stages reliably.

3.3. Proposed full swing XOR gate

This subsection details about the proposed XOR gate to achieve full swing operation. It acts as one of the basic modules for the realization of three full adder designs and the performance of the designed adders are investigated under full swing XOR gate as one of the modules.

The proposed XOR gate uses 4T to provide full swing in the output. The design of XOR gate using GDI logic without and with full swing is shown in Fig 3.

The goal is to reduce the circuit complexity and to achieve faster cascaded operation. The techniques presented in the literature directly use supply rail V_{DD} for strong '1' and V_{SS} for strong '0'.

But the proposed design does not use supply rails either GND or V_{DD} for obtaining the perfect output. It uses input, but only with proper biasing of a necessary transistor, which may be either PMOS or NMOS.

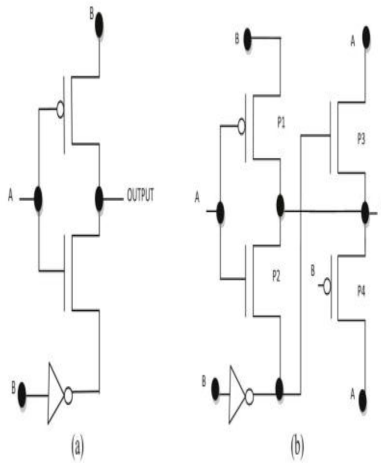

Fig.3. XOR gate (a) using GDI logic and (b) proposed design

For AB = 00, transistor P1 (PMOS), P3 (NMOS) and P4 (PMOS) conduct. The P3 transistor is responsible for delivering strong ‘0’.Likewise, another case when AB = 10, transistor P2 (NMOS), P3(NMOS) and P4 (PMOS) work for the given input, in which P4 passes strong ‘1’ to the output. Whereas in other cases, namely AB = 01 and 11, the transistors P3 and P4 do not change the output potential. Hence, the correct output for XOR gate is attained with the proposed design.

4. THREE FULL ADDER DESIGNS

The design of GDI full adder with full swing can be made possible with the help of full swing gates such as AND, OR and XOR discussed in the previous section. This design completely eliminates the swing restoration buffers that results in improvement in the performance. Three possible full swing GDI full adders are designed by rewriting the full adder design expression Eqs. (1) and (2). The full adder’s Sum and C_{out} expressions are given in Eqs. (3) and (4), respectively.

$$Sum= C_{in}\ (A\ XOR\ B) + C_{in}\ (A\ XNOR\ B) \quad (3)$$

$$C_{out}= (A\ XOR\ B)C_{in} + (A\ XOR\ B)A \quad (4)$$

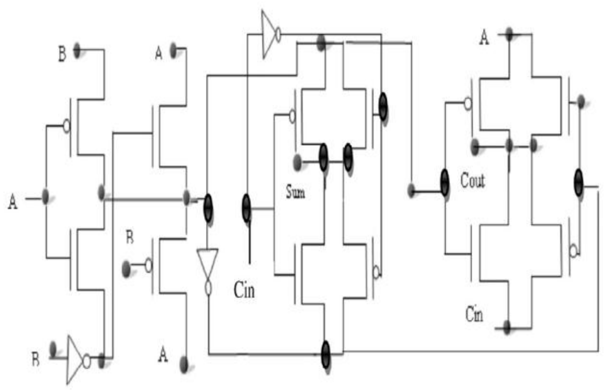

Fig.4. Design 1 Full adder

Design 1 uses XOR output as an intermediate result. Sum output can be attained by multiplexing the XOR and its inverted version XNOR through C_{in} input. C_{out} is obtained by multiplexing the inputs A and C_{in} whose output is controlled by the selection input. The presence of inverter on the critical path increases the delay of the whole circuit. This design is simple and requires a total of 18 transistors for realizing the full adder function.

Design 2 The Sum and C_{out} expressions are represented in Eqs. 5 and 6, respectively.

$$Sum= A\ XOR\ B\ XOR\ C_{in} \quad (5)$$

$$C_{out}= C_{in}\ (A\ AND\ B) + C_{in}\ (A\ OR\ B) \quad (6)$$

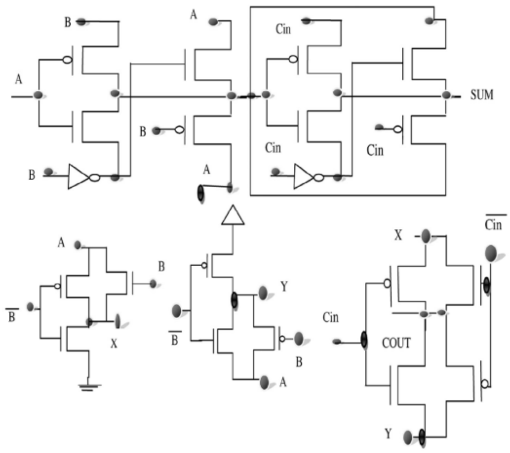

Fig.5. Design 2 Full adder

C_{out} function can be realized with the help of AND and OR gates. AND and OR gates are designed based on F1 and F2, respectively. Multiplexing the AND and OR operation through Carry input C_{in} helps in C_{out} realization. The XOR operation on the inputs A, B and C_{in} achieves Sum function. It requires total 22 transistors.

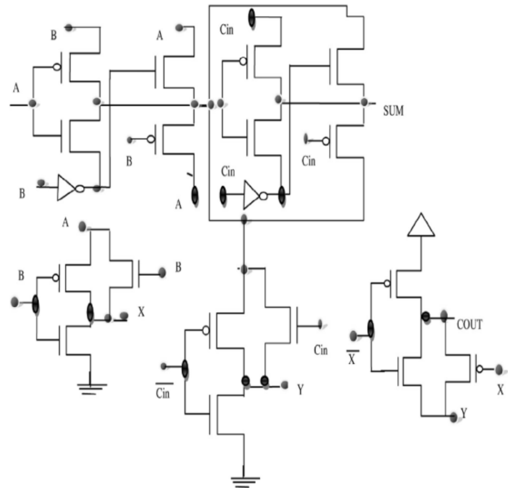

Fig.6. Design 3 Full adder

Design 3 It is designed by considering the XOR, AND and OR gates and the Sum and C_{out} design expressions are given in Eqs. (7) and (8).

$$Sum= A\ XOR\ B\ XOR\ C_{in} \quad (7)$$

$$C_{out}= A\ AND\ B + (A\ XOR\ B)\ C_{in} \quad (8)$$

Sum output can be achieved by XORing the inputs A, Band C_{in}. The output C_{out} is obtained with the help of AND and OR followed by XOR gate. The realization of AND and OR gate can be done with the help of full swing F1 and F2 gates.

The GDI based F1 and F2 enables the implementation of AND and OR with only 3 transistors whereas CMOS needs 6 transistors for achieving the same. The intermediate XOR gate output is used for computing C_{out} output. So totally, 23 transistors are needed for designing a full adder. The proposed full adder based on Design 1, Design 2 and Design 3 are shown in the above Fig 4, 5, 6.

5. RESULT ANALYSIS

Table II. Comparison of Full adders

Full Adder	Transistor Count	Average Power (µw)	Delay	
			Sum (ps)	C_{out} (ns)
Design 1	18	0.55164	993.5	1.496
Design 2	22	0.052718	991.3	1.990
Design 3	23	0.652367	992.3	1.475

(a) Design 1 is a best possible candidate for the applications in which minimum transistor count and low power is a design requirement.

(b) The Design 2 offers minimum delay, so it can be suitable for battery operated and real-time applications. It has slightly increased in transistor count compared with Design 1.

(c) Design 3 lies midway between Design 1 and Design 2, and offers lower delay than Design 1.

From the obtained results, it can be concluded that all three designs operate with less energy consumption than existing adders taken for comparison. Hence, these designs can be suitable for realizing energy efficient arithmetic applications.

6. CONCLUSION

In this work, three full adder designs that use as few as twenty transistors per bit are proposed. The design adopts full swing XOR, AND and OR gates to alleviate the threshold voltage problem and to enhance the driving capability for cascaded operation. The enhanced driving capability also facilitates lower voltage and faster operation which leads to power consumption. The proposed designs are simulated using the SPICE simulation tool at 45 nm technology. The comparison is done in terms of power consumption, propagation delay, and transistor count.

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