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Design and Analysis of Low Power High Speed Hybrid logic 8-T Full Adder Circuit

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ABSTRACT

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This addition module is also the core of other arithmetic operations such as subtraction, multiplication, division and address generation. The prime objective of this project is to design a full-adder having low-power consumption and low propagation delay which may result in the efficient implementation of modern digital systems. This model is referred as "hybrid" because of the combination of two different design logic styles namely CMOS logic and pass transistor logic. Performance parameters such as power, delay and hence energy were compared with the existing designs such as complementary CMOS logic full adder. In the existing hybrid systems, over 28 transistors were used. While the optimized hybrid full adder circuit reduces this count to 8 transistors, it still obtains better energy efficiency. Further the proper working of proposed full adder is verified by applying it in a Ripple carry Adder circuit.

1. INTRODUCTION

1.1 Need for Low Power

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. Now a day's power is the primary concern due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption.

The motivations for reducing power consumption differ application to application. In the class of micro-powered battery operated portable applications such as cell phones, the goal is to keep the battery lifetime and weight reasonable and packaging cost low. For high performance portable computers such as laptop the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation. Finally For the high performance non battery operated system such as workstations the overall goal of power minimization is to reduce the system cost while ensuring long term device reliability.

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability; power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Several factors have contributed to this trend.

Perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices and wireless communications systems which demand high-speed computation and complex functionality with low power consumption. In these applications, average power consumption is a critical design concern. From the environmental viewpoint, the smaller the power dissipation of electronic systems, the lower the heat pumped into the rooms, the lower the electricity consumed and hence the lower the impact on global environment.

1.2 Need for Energy efficient Adders

Adders are the most important components used in most of the Digital signal processors for real time applications. Adders are also used in the architecture of other arithmetic operators like Subtractors, Multipliers, shifters, MACs, etc. Many Adder architectures have been proposed by various researchers over the years. Even today the researches on Adder architectures are finding a major interest for achieving energy efficient devices. The survey on conventional adder architectures [3, 5-9] have proved there is a lot more scope for optimization. One method of optimization is by using different logic styles for different parts of the design instead of using the same logic style throughout the design. This method of designing with different logic styles in various parts of the same circuit is called Hybrid circuit. Various hybrid architectures were surveyed for reference [1, 2 and 4].

This paper presents a Hybrid full adder circuit consisting of two different logic styles namely CMOS logic and Pass transistor logic. This method has lesser power consumption, and hence energy efficient. The remaining of this paper is organized as follows. Section II presents the overview of proposed hybrid full adder circuit, the two different logic styles and the reason behind using them in this circuit. Section III presents the working principle of the proposed design with an example and the analysis of obtained results using Tanner Tool of 180nm Technology. Section IV draws the most relevant conclusions of this work.

2. PROPOSED HYBRID FULL ADDER CIRCUIT

2.1 Overview of existing systems

Full adders, being one of the most fundamental building blocks of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years. Different logic styles, each having its own merits and bottlenecks, was investigated to implement1-bit full adder cells. The designs,

reported so far, may be broadly classified into two categories: 1) static style 2) dynamic style. In the existing system, full-adder has to obtain an intermediate signal and its complement, which are then used to drive other blocks to generate the final outputs. The overall propagation delay and the power consumption of the full-adder depend on the delay and its complement generated. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path**.**

In most hybrid techniques, XOR, and XNOR functions were simultaneously generated by pass transistor logic module by using only six transistors. CMOS module produces full swing outputs of the full adder but at the cost of increased transistor count and decreased speed. Although the hybrid logic styles offers promising performance, most of these hybrid logic adders suffered from poor driving capability issue and their performance degrades drastically in the cascaded mode of operation if the suitably designed buffers are not included.

2.2 Overview of the proposed system

In this proposed system Pass Transistor Logic and CMOS logic are used hence hybrid adder. In the proposed work, consideration is given to the sizing of the MOS transistors during the initial design step. A low transistor count full adder cell using the new XOR cell is also presented. A PTL based 3-transitors XOR and XNOR circuits presented in had full output voltage swing and better driving capability. To compare the performance of new circuit and test their driving capability, an adder circuit is built with the proposed XOR and XNOR circuits.

An XOR/XNOR function with low circuit complexity can be achieved with only 3 transistors in PTL. It uses only six transistors to produce both an XOR and the complementary XNOR function. The circuit has full voltage-swing and negligible static power dissipation. The entire model is divided into 3 modules, each module performing a specified task. Here the propagation delay and power consumption is reduced.

2.3 Hybrid technique of the proposed system

2.3.1 Pass transistor logic

The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications. The low power pass transistor logic and its design and analysis procedures were reported. The advantage of PTL is that only one PTL network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in smaller number of transistors and smaller input loads, especially when NMOS network is used. Moreover, VDD-to GND paths, which may lead to short-circuit energy dissipation, are eliminated. As the designs with fewer transistor count and lower power consumption are pursued it becomes more and more difficult and even obsolete to keep full voltage swing operation. In pass transistor logic, the output voltage swing may be degraded due to the threshold loss problem. That is, the output high (or low) voltage is deviated from the VDD (or ground) by a multiple of threshold voltage. The reduction in voltage swing, on one hand, is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation such as ripple carry adder. At low operation, the degraded output may even cause circuit malfunction. A formal design procedure for realizing a minimal transistor CMOS pass network XOR cell is presented.

The advantages of pass transistor based realization are ratio less, lower area due to smaller number of transistors and lesser power dissipation because of no static power and short circuit power dissipation. Some of the disadvantages of pass transistor logic are higher delay and multi threshold voltage drop. Pass transistor logic family is used to overcome the limitations of pass transistor circuits. Some of the techniques are:

Insertion of buffers to avoid long delay of a chain of pass transistor logic.

Use of swing restoration circuit to overcome multi-threshold voltage drop (vout = vdd-vtn).

Use of dual rail logic to generate complementary control signals.

Most of full adder designs are based on three module implementation i.e. XOR, sum, carry modules. The 4-Transistor XOR (XNOR) module is used to design pass transistor logic based full adder. But this type of design raises severe threshold voltage loss problems. The signal degradation in the output causes signal degradation in the further modules. Finally the signal degradation in the circuit causes a multi-threshold loss problem at the output stage. These multi-threshold loss problems can be reduced by using complementary outputs. The complementary outputs are obtained by using 5-Transistor XOR-XNOR design.

2.3.2 The CMOS logic

In all static CMOS circuits, a rising output transition is caused by one of the pMOS branches, where a falling output transition is always caused by one of the nMOS branches. The delay associated with a certain transition is dictated by the strength (or weakness) of the corresponding branch. Thus, with the help of some simulations, the designer can identify which branches are responsible for particular outputs. This will enable the designer to modify the dimensions of only the relevant transistors. The pMOS transistors, due to the lower mobility of holes, have a gain factor that is 2 to 3 times lower than that of an nMOS transistor. For the same current driving capacity the pMOS transistor should have channel width that is roughly 2 to 3 times wider than an nMOS transistor. Larger transistors have larger current driving capability, making them faster. The problem is that larger transistors also have higher input capacitances and higher drain parasitics which slows down overall operation speed. Transistors within the same branch are usually drawn side-by-side on the same active area. Thus, they should have the same size to simplify the layout. For some common blocks there are many different alternatives with varying advantages and disadvantages. As

an example, XOR and MUX type circuits are hard to realize in standard CMOS logic whereas in Pass transistor logic their realization is quite simple. A very interesting design style for efficient layouts is the branch based logic style. The branch based logic style is a special case of the standard static CMOS designs where both the nMOS and pMOS block of the circuit are designed using parallel branches of series-connected transistors between the VDD (or GND) and the output node.

2.3.3 Hybrid Designs Using XOR and XNOR

All hybrid designs use the best available modules implemented using different logic styles or enhance the available modules in an attempt to build a low power full-adder cell. Generally, the main aim is to reduce the number of transistors in the adder cell and consequently to reduce the number of power dissipating nodes. This is achieved by utilizing intrinsically low power consuming logic styles like TGA, TFA or simply pass-transistors. There are three main components to design a hybrid full adder circuit. These are XOR or XNOR, Carry generator and Sum generator. Hybrid full adder as shown in Figure has been designed with pass logic circuit cogenerates the intermediate XOR - XNOR and hence improves outputs. The carry generator module of hybrid full adder is a complementary CMOS logic style based MUX. In this circuit, worst case delay problems of transitions from 01 to 00 and from 10 to 11 are solved by adding two series p-MOS and two series n-MOS transistors respectively. Although this modification improves the speed of XOR/XNOR circuit, these additional transistors increase the power consumption of the full adder cell.

To produce sum, hybrid uses another XOR circuit which is implemented with pass transistors. The output inverter restores the output voltage level and improves the driving capability for cascading. It uses 26 transistors having a full swing logic, balanced output and good output drivability at low voltage. Another hybrid designed full adder is a combination of low power transmission-gates and pseudo n-MOS gates as depicted in Figure. XOR gate consists of a pMOS transistor and an nMOS transistor that are connected in parallel, which is a particular type of pass-transistor logic circuit. There is no voltage drop at output node but it requires twice the number of transistors to design similar function.

A novel 8-transistor XOR–XNOR based Full adder circuit that generates XOR and XNOR outputs simultaneously. This circuit provides a full voltage swing (i.e., 0V for logic 0 and 1.8V for logic 1) at low supply voltage. The reported XOR–XNOR Full adder circuit is based on complementary pass-transistor logic using only one static inverter instead of two static inverters as in the regular CPL style XOR circuit.

The first half of the circuit utilizes only NMOS pass transistors for the generation of the XOR and XNOR outputs. The cross-coupled PMOS transistors are connected between XOR and XNOR output to alleviate threshold problem for all possible input combinations and reduce short-circuit power dissipation. The circuit is inherently fast due to the high mobility NMOS transistors and the fast differential stage of cross-coupled PMOS transistors. It indicates the functioning of the XOR/XNOR circuit.

3. WORKING PRINCIPLE OF FULL ADDER CIRCUIT

The proposed full adder circuit is represented by three blocks Module 1 and module 2 are the XNOR modules that generate the sum signal (SUM) and module 3 generates the output carry signal (Cout).

3.1 Carry generation module

In the proposed circuit, the output carry signal is implemented by the transistors Mp7, Mp8, Mn7, and Mn8. The input carry signal (*C*in*)* propagates only through a single transmission gate (Mn7 and Mp7), reducing the overall carry propagation path significantly.

3.2 Operation of the proposed full adder

The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B', which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. But it has some voltage degradation problem, which has been removed using two pass C transistors Mp3 and Mn3. Analyzing the truth table of a full adder, the condition for *C*out generation has been deducted as follows:

If, A = B, then Cout = B; else, Cout = Cin.

Let A=0; B=1; Cin=0;
Module 1: A 'XNOR' B = 0 (S1);
Module 2: 'NOT' (S1) =1(S2);
S2 'XNOR' Cin = 0,
which is the Cout
Module 3: S1 'XNOR' Cin : 1,
which is the SUM

The parity between inputs A and B is checked by A _ B function. If they are same, then Cout is same as B, which is implemented using the transmission gate realized by transistors Mp8 and Mn8. Otherwise, the input carry signal (Cin) is reflected as *C*out which is implemented by another transmission gate consisting of transistors Mp7 and Mn7.We use thin and thick gates for CMOS and transistor gates respectively to reduce the power consumption and propagation delay.

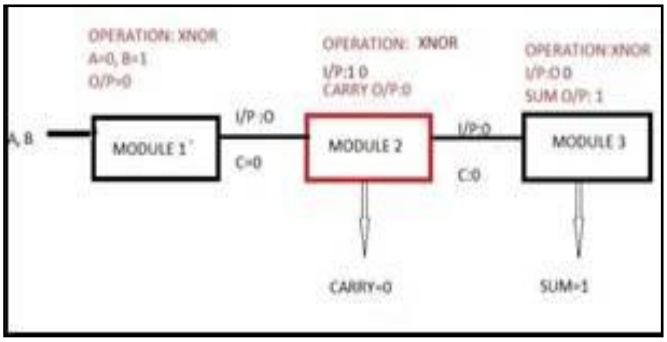

Fig.1. Working of the proposed full adder

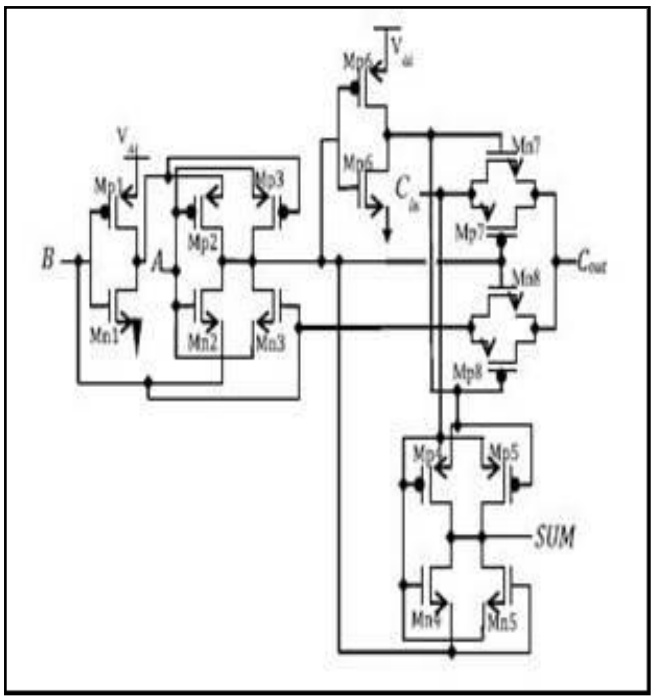

Fig.2. Schematic of proposed full adder

3.3 Working of the optimized full adder circuit

The working principle of the optimized full adder is presented below. The working is divided into 3 modules and each of these modules performs its intended operation. This optimized circuit is a hybrid full adder which combines PTL logic and CMOS logic.

3.4 Carry and sum generation modules

In the module1, XOR logic is used. 2 inputs are given to the circuit A and B. These two inputs are XORed and the output is considered to be S1. To consider an example say A=0, B=1 then A XOR B= 1.

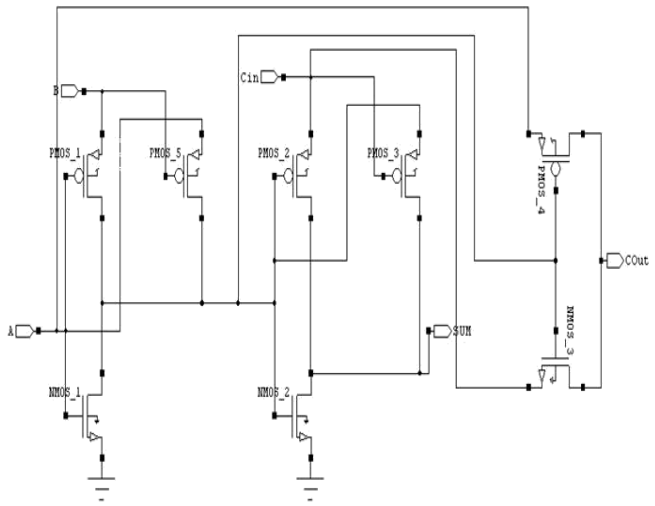

Fig.3. Schematic of the optimized Full adder circuit

In the module 2 XOR logic is used .The S1 from the first module and Cin is given as the input and here the operation is S1 XOR Cin the output is the SUM for the given set of the problem. If Cin =1, then S1 XOR Cin =0 (SUM).

- **A=0, B=1, Cin=1;**
- **Module 1: A 'XOR' B = 1 (S1);**
- **Module 2:Cin 'XOR' (S1) =0(Sum);**
- **Module 3: MUX operation**

S1, Cin, selection line (SL)=A

CONDITION: "If A=0, Cout=Cin,

If A=1, Cout=S1"

Hence output is: carry(Cout)=1 ,sum=0.

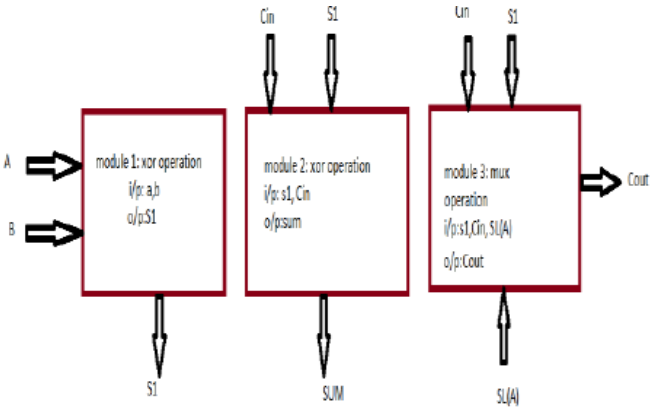

Fig.4. Working of the optimized full adder

In the module 3 MUX logic is used thus we have a 2*1 mux logic that is two inputs and one output, a selection line is also used the inputs are SI and Cin the input A is the selection line which is denoted by SL. The output of this MUX operation is the carry. Thus the carry is 1 which is the Cout. The condition for this carry generation is: ***"If A=0, Cout=Cin, If A=1, Cout=S1"***

3.5 Results and Analysis

Table 1. Comparative Analysis of Full Adders

Methods	No of transistors	Power (mW)	Propagation delay (sec)	Energy (mJ)
Conventional CMOS	28	30	1.29	38.7
Hybrid full adder	16	18.18	1.17	21.3
Optimized Hybrid full adder	8	12.73	1.29	16.4

The table 1 shows the comparison among the conventional CMOS full adder, the hybrid full adder and the optimized full adder we have calculated number of transistors used in all the three from which we can infer that the proposed optimized full adder uses only 8 transistors while the hybrid full adder system uses 16 and the conventional uses 28. We have

calculated the power consumed and propagation delay from which we have calculated the power delay product which is nothing but the energy and hence from the above details we can conclude that the energy is reduced up to 23% in the optimized full adder.

3.6 *Application of proposed Hybrid full adder*

The proper working of the proposed hybrid full adder design has been verified by applying the circuit in a Ripple Carry Adder (RCA). Ripple Carry Adders were the conventional 4 bit adders used for many arithmetic operations. They are known for their simple architecture. The drawback associated with RCA is the propagation delay associated with the propagation of carry signal in between full adder blocks.

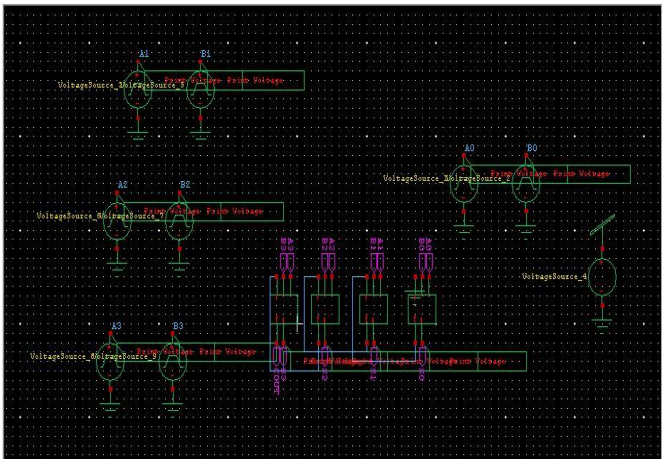

Fig.5. Schematic of the Ripple Carry Adder

This Figure shows the schematic view obtained from S-Edit of RCA from Tanner Tool. The different full adders namely conventional proposed hybrid full adders are called in correspondingly for different methods. Similar results were achieved for RCA circuit analysis also. The results are displayed in the following table.

Table 2: Comparative Analysis of Full Adders

Methods	No of transistors	Power (mW)	Propagation delay (sec)	Energy (mJ)
Conventional CMOS RCA	65	90	2.16	194.4
Hybrid full adder_RCA	34	75	2.05	153.75
Optimized Hybrid full adder_RCA	26	70	2.02	141.4

The table 2 shows the comparison among the conventional CMOS RCA, the hybrid full adder_RCA and the optimized full adder_RCA. There is a clear reduction in the number of transistors. We have calculated the power consumed and propagation delay from which energy has been analysed, resulted in an energy reduction by 27.2% compared to conventional circuit.

4. CONCLUSION

In this work, a hybrid full adder circuit and a ripple carry adder circuit using the proposed hybrid full adder circuit are designed and analyzed using TANNER SOFTWARE. This full adder is compared with the conventional CMOS based full adder. Hybrid Full adder is designed with two different logic designs namely CMOS logic and Transmission gate logic. Further optimization of the proposed full adder is also done for better results by replacing the transmission gates with the pass transistor logic. These systems are analyzed for power consumption, propagation delay and hence energy (power delay product), using T-SPICE. From these computations, it is concluded that the optimized full adder is energy efficient when compared with the hybrid full adder circuit. The energy is reduced up to 23%.

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