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Implementation of High Performance Carry Save Adder Using Domino Logic

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ABSTRACT

In most of the modern day computers adder is an essential circuit. The primary requirement of adder is that, it is fast and efficient in terms of power consumption and chip area. Here we design a CSA (Carry Save Adder) using domino logic. CSA can be designed using two full adder circuits. The circuit is implemented in domino logic by switching PMOS to off state and NMOS to on state and adding a static inverter at the output. Domino Logic with CSA gives better result in terms of power dissipation, area, speed and reduction in transistors count required. To design an efficient integrated circuit in terms of area, power and speed has become a challenging task in modern VLSI design field .Performance analysis was carried out between multiplier using Carry Propagate Adder(CPA) and by using Carry Save Adder.

Keywords: Carry Save Adder, Carry Propagate Adder, Domino Logic Circuits, Delay and Power Consumption.

1. INTRODUCTION

The high performance and low power consumption has become important in today's VLSI circuit design. The exponential growth of portable electronic devices like laptops, multimedia and cellular device, research efforts in the field of low power VLSI systems have increased. Now a day's low power consumption along with minimum delay and area requirements is one of important design consider for IC designers. There are three major source of power consumption in VLSI circuits:

1) Switching power due to charge and discharge of capacitances.
2) Short circuit power due to current flow from power supply to ground with simultaneous function of p-network and n-networks.
3) Static power due to leakage currents.

The need for higher performance has used a Domino circuits where conventional static CMOS circuits may not meet the low critical path delay.

Hybrid CMOS logic styles have a higher design freedom to the desired performance. Hybrid full adder has higher speed, less power consumption and higher performance. Full adders are fundamental in various circuits which is used for performing arithmetic operations such as addition, subtraction, multiplication, address calculation, comparator and MAC etc. Enhancing the performance of the full adders can significantly affect the whole system performance.

There are two logic approaches for designing a full adder first is static style and second is dynamic style. Static full adder are more reliable, simpler and low power than dynamic ones but dynamic full adder are more fast and some times more compact than static full adder.

Recent technology scaling and use of various logic families provides techniques to achieve power consumption at the cost of performance. Power, speed and robustness are so critical to leading edge designs that they need to be taken care of each level of design. The choice of logic styles is a very important constraint at the circuit level. Logic styles differ in terms of energy, delay, area and robustness. Because every design requires compromises and trade-offs, designers need to pick and choose circuits from different points on an energy delay-robustness envelope to meet each circuit need. Among other things, meeting the needs of future computing will require logic style that satisfies high-performance, low-power, high robustness in the form of noise and variability, ease of implementation and verification. In addition to that, we want to use logic styles that are compatible for all types of logic implementation for further improvement in robustness. The objective of this research work is to modify and improve domino logic that can provide further improvement in power consumption, performance, speed and area overhead.

- The main objective is to reduce the delay, area and power consumption.
- Number of transistors required for circuit design gets reduced.
- The performance of the system is high, hence the speed increases.

2. DOMINO LOGIC

Domino logic is a clocked logic family which means that every single logic has a clock signal present. When the clock signal turns low, node N0 goes high, causing the output of the gate to go low. The mechanism for the gate output to go low once it has been driven high. The operating period of the cell when its input and output are low is called the recharge phase. The next phase, when the clock is high, is called as evaluate phase. The evaluate phase is the functional operating phase in domino cells, with the recharge phase enabling the evaluate

phase to occur. The application of the clock signal ensures that the critical path in domino cells only traverses through cells in the evaluate phase. Since the domino cell only switches from a low to a high direction, there is no need for the inputs to drive any pull-up PMOS transistors. The lack of a PMOS transistor means that the effective transistor width has loads down a previous stage of logic, for a particular current drive, favors domino over static logic. This is critical since the high speed ensures that a speed advantage can be gained without loading down the cell greatly.

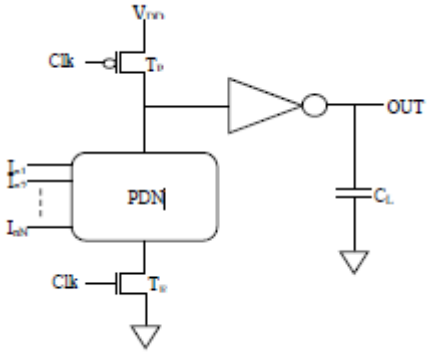

Fig.1. Domino CMOS Logic

3. DOMINO FULL ADDER

Full adder cell realization uses 27 transistors as shown in Figure.2.It has lower delay as compared to static adder circuit having 28 transistor counts. It is based on the 3 transistor implementations of XOR and XNOR functions presented in, pass transistors and transmission gates. This circuit has several advantages, First, it reduces the number of transistor count which decreases the cell area as well as delay. Second, It balances the delays of generating XOR and XNOR, which lead to fewer glitches at the output. The output of full adder cell SUM and COUT can be produced using intermediate signal K = (B⊕C)' or K' = B⊕C.

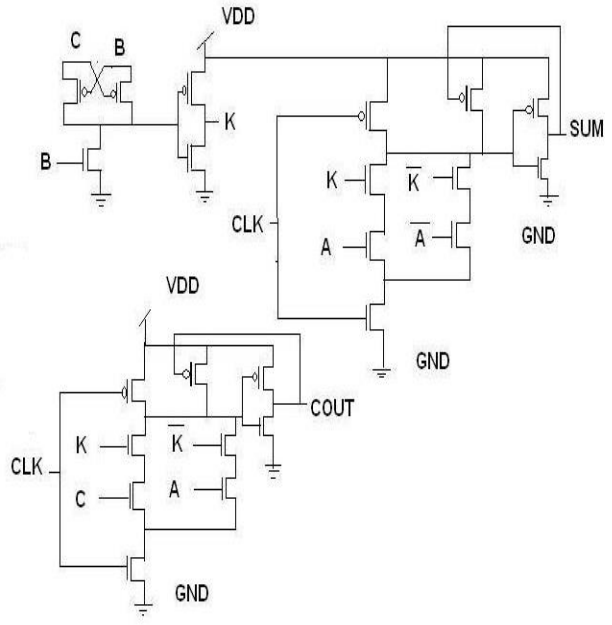

Fig.2. 27 Transistor 1-bit domino full adder

4. CARRY PROPAGATE ADDER

It is possible to create a logical circuit using many full adders to add N-bit numbers. Each full adder inputs is Cin, which is the Cout of the previous adder. This kind of adder is called a carry propagate adder shown in figure 3. Each carry bit "ripples" to the next full adder. The layout of a carry propagate adder is simple, which allows for fast design time. The carry propagate adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit.

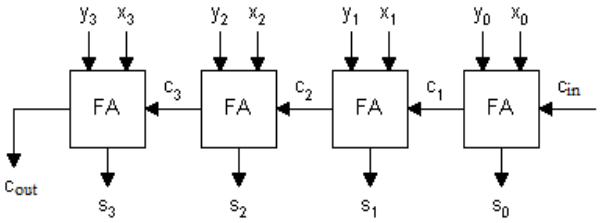

Fig.3. Carry Propagate Adder

CPA has the simplest structure with the smallest area and power consumption, but it is not very efficient when large number of bits are used and delay increases linearly with the bit length. Delay from carry-in to carry-out is more important than from X to carry-out or from carry-in to SUM, because the carry-propagation chain will determine the latency of the whole circuit for a Carry Propagate Adder. Table 1 shows the truth table of a binary full adder. A and B are the adder inputs Cin is the carry input, S is the sum output, and Cout is the carry output based on this truth table.

5. CARRY SAVE ADDER

Carry save adder is consists of three or more n-bit binary numbers. Carry save adder is similar as full adder. Here we are computing sum of 3-bit binary numbers, so we take 3 full adders at first stage. Carry save unit consists of 6 full adders, each of which computes single sum and carry bit based only on the corresponding bits of the two input numbers. Let X and Y are two 3-bit numbers and produces partial sum and carry as S and C as shown in the Table 1.

Si = Xi xor Yi

Ci = Xi and Yi

Table 1. Carry save Adder Computation

X: 1 0 0 1 1
Y: 1 1 0 0 1
Z: + 0 1 0 1 1

S: 0 0 0 0 1
C: + 1 1 0 1 1

Sum: 1 1 0 1 1 1

The addition is then computed as:
1. Shifting the carry C left by one place.
2. Placing a 0 in front (MSB) of the partial sum sequence S.

3. Finally, a carry propagate adder is used to add these Two sequences together and computing the resulting sum.

5.1 Operation of CSA

CSA consists of 2 pair of blocks with each block consisting of a pair of carry propagate adders and two multiplexers controlled by incoming carry signal. One is to select one of the two carry outputs and the other one is to select one of two n bit SUMs. The carry propagation logic of each block of CSA has two paths: one has '0' as its CARRY input to the first stage and other has '1' as its CARRY input. Carry-out will be the same as Carry-in for every stage because each carry propagation logic get propagates. Carry-in to Carry-out has no change. Hence, every circuit will be evaluated in the preferential skew direction. This has the largest propagation delay because Carry-in goes through all stages in the path.

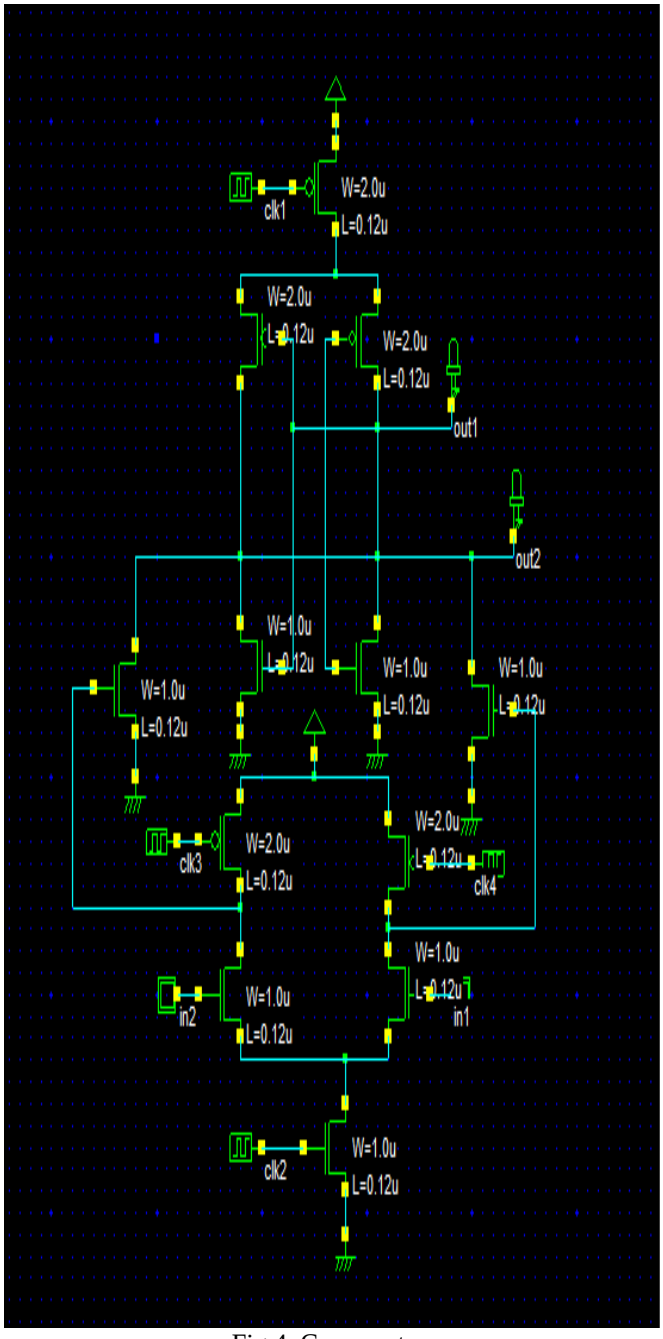

Fig.4. Comparator

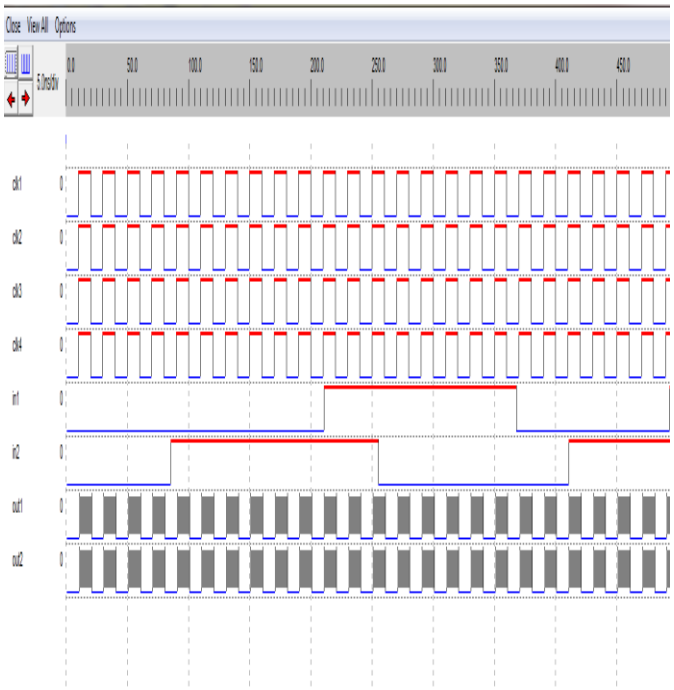

Fig.5. Simulation Output of 3- Bit Comparator

6. COMPARATOR

Comparator is a fundamental building block in most of the analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, high-speed, low power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies with low power voltages. When we consider the fact of threshold voltages of the devices have not been scaled at the same time for the supply voltages of the modern CMOS processes. Designing high-speed comparators is more challenging when the supply voltage is smaller. The technologies has achieved high speed, larger transistors are required to compensate the reduction of power supply, which reduces the area and power is needed. Low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods, ,current-mode design and using dual-oxide processes, which can handle high supply voltages have been developed to meet the low-voltage design challenges.

Boosting and bootstrapping are two techniques used in augmenting the power supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock, removes the threshold voltage required such that body driven MOSFET operates as a depletion-type device. A 1-bit quantizer for sub-1V modulators is used. Advantages, the body driven transistor suffers from smaller transconductance compared to its gate-drive counterpart while the fabrication process, such as deep n-well is required to have both NMOS and PMOS transistors operating in the body-driven configuration. Developing new circuit structures which avoid the transistors between the supply rails is preferable for low-voltage operation, if they do not increase the circuit complexity.

7. 3-BIT CARRY SAVE ADDER

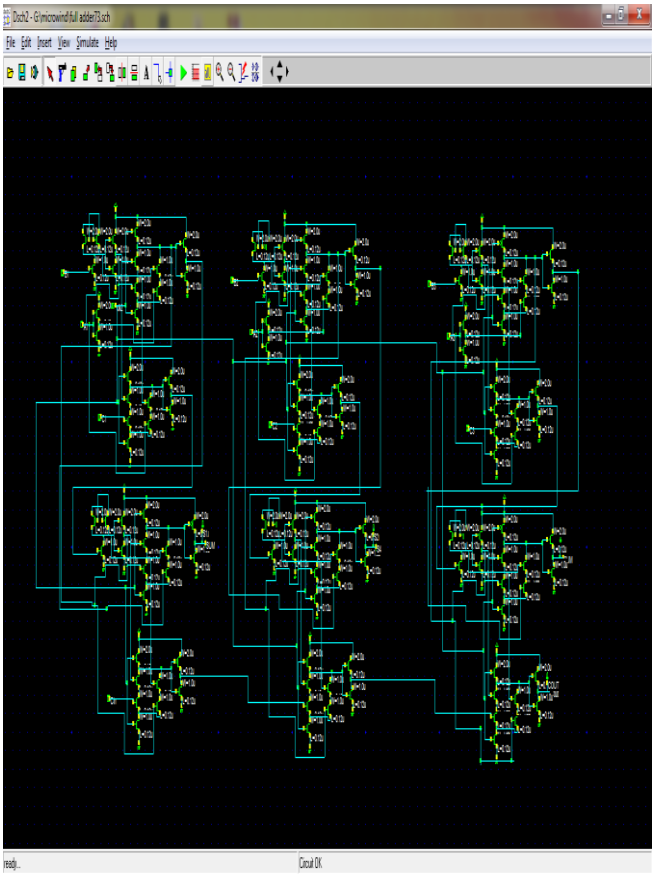

Fig.6. 3-Bit Carry Save Adder

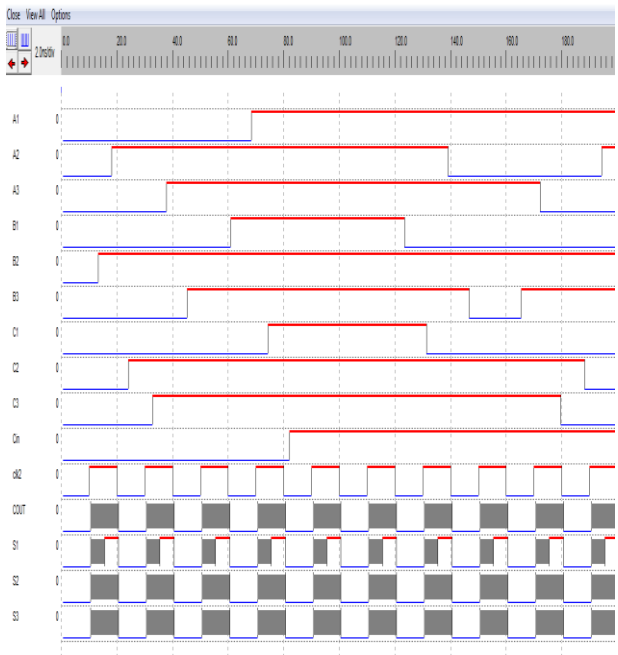

Fig.7. Output of 3- Bit Carry Save Adder

8. CONCLUSION

We have designed the domino logic based full adder, carry propagator adder, carry save adder. We have shown the power is reduced, delay is reduced and the number of transistors required for this construction is also reduced i.e., area is reduced. We have also designed comparator using domino logic. Dynamic Comparator with low – voltage, low-power capability will reduced delay. This system is simulated by using MICROWIND tool and the output simulated waveform is analysed.

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