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A High Speed and Power Efficient Voltage Level Shifter for Dual Supply Applications

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ABSTRACT

This brief presents a fast and power-efficient voltage level- shifting circuit capable of converting extremely low levels of input voltages into high output voltage levels. The efficiency of the proposed circuit is due to the fact that not only the strength of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit. Post layout simulation results of the proposed circuit in a 0.18-µm technology demonstrate a total energy per transition of 157 fJ, a static power dissipation of 0.3 nW, and a propagation delay of 30 ns for input frequency of 1 MHz, low supply voltage level of VDDL = 0.4 V, and high supply voltage level of VDDH = 1.8 V.

Keywords: Power-efficient voltage level- shifting circuit and Pull-up device.

1. INTRODUCTION

One of the most effective ways to reduce dynamic and short-circuit power consumption of digital circuits is lowering the value of the power supply voltage [1]–[3]. On the other hand, reducing the supply voltage increases the propagation delay of the circuits. Moreover, less headroom in analog circuits decreases signal swings and therefore increases the sensitivity to noise. Hence, in moderate-speed mixed- signal circuits or in digital circuits where different parts operate at different speeds, dual-supply architectures are introduced in which a low voltage (i.e., V_{DDL}) is supplied for the blocks on the noncritical paths while a high supply voltage (i.e., V_{DDH}) is applied to the analog and the high-speed digital blocks [2], [3]. In a system with dual supply voltages, level-shifting circuits are needed to convert the lower logic levels into the higher ones to provide correct voltage levels for the next digital blocks. In order to alleviate the degradation of the overall performance of the circuit, the required level shifters must be designed with minimum propagation delay, power consumption, and silicon area. In addition, in order to have more power saving in the low-supply blocks, the employed level shifters must be able to convert the extremely low values of V_{DDL} to even lower than the threshold voltage of the input transistors. Hence, in this brief, a fast and power-efficient voltage level shifter is proposed, which is able to convert extremely low values of the input voltages.

The rest of this brief is organized as follows. In Section II, some of the recently reported high-performance voltage level shifters are reviewed. The proposed circuit is introduced in Section III. Section IV presents the simulation results of the designed circuit verifying the efficiency of the proposed structure. Finally, this brief is concluded in Section V.

2. DESIGN METHODOLOGY

The presentation of fast and power-efficient voltage level- shifting circuit capable of converting extremely low levels of input voltages into high output voltage levels. The efficiency of the proposed circuit is due to the fact that

not only the strength of the pull-up device is significantly reduced when the pull-down device is used to pulling the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit.

3. VOLTAGE LEVEL SHIFTING METHOD

One of the conventional level-shifting architectures is shown in Fig. 1(a). The operation of this circuit is as follows. When the input signal IN is "High = VDDL," MN1 and MN2 are ON and OFF, respectively. Therefore, MN1 tries to pull the node Q1 down. Consequently, MP2 is gradually turned on to pull the node Q2 up to VDDH and to turn MP1 off. Similarly, when the input signal is changed to "Low = VSS," the operation is forced to reverse states. It is noticeable that, in this structure, there is a contention at the nodes Q1 and Q2 between the pull-up devices (i.e., MP1 and MP2) driven with VDDH and the pull- down devices (i.e., MN1 and MN2) driven with VDDL. As a result, when the voltage difference between VDDL and VDDH is high and particularly when the input voltage is in sub threshold range, this circuit will no longer be able to convert the voltage levels. This is because the currents of the pull-down transistors are smaller than those of the pull-up devices.

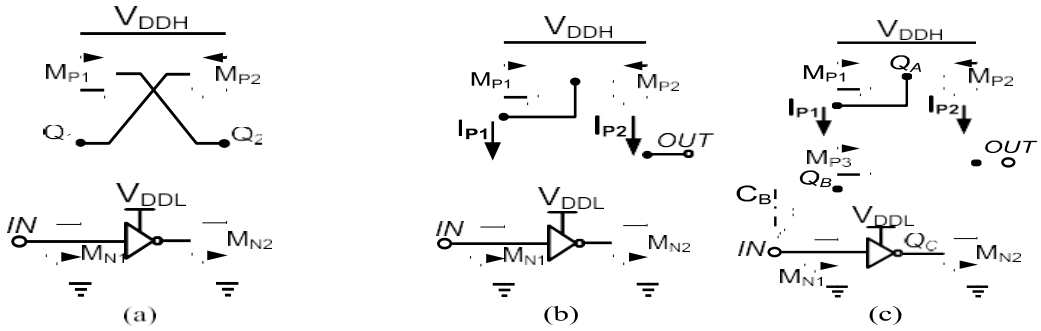

Fig. 1. Schematic of the (a) conventional level shifter, (b) level shifter with a semi-static current mirror, and (c) level shifter with a dynamic current mirror (Wilson current mirror) [5].

4. CONVENTIONAL VOLTAGE LEVEL SHIFTER

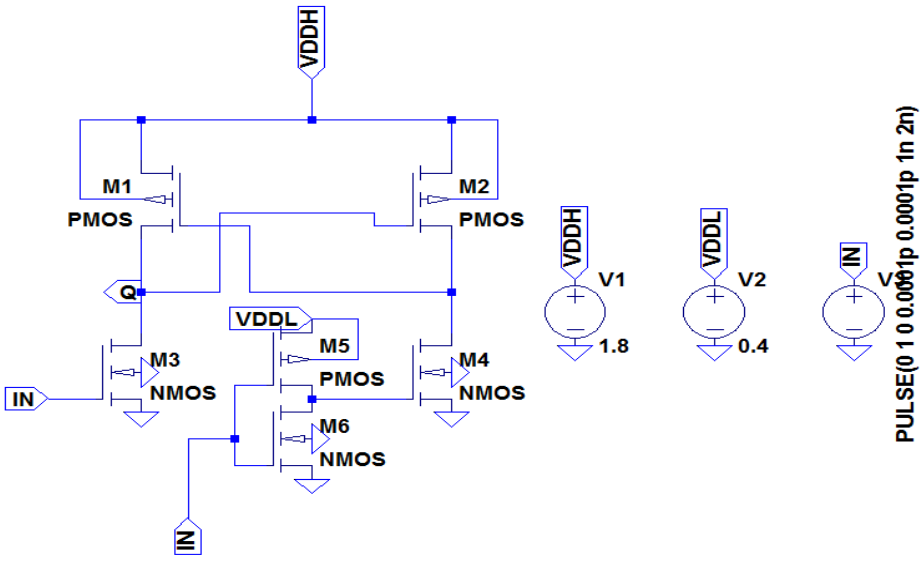

Fig. 4.1. Schematic diagram of conventional voltage level shifter

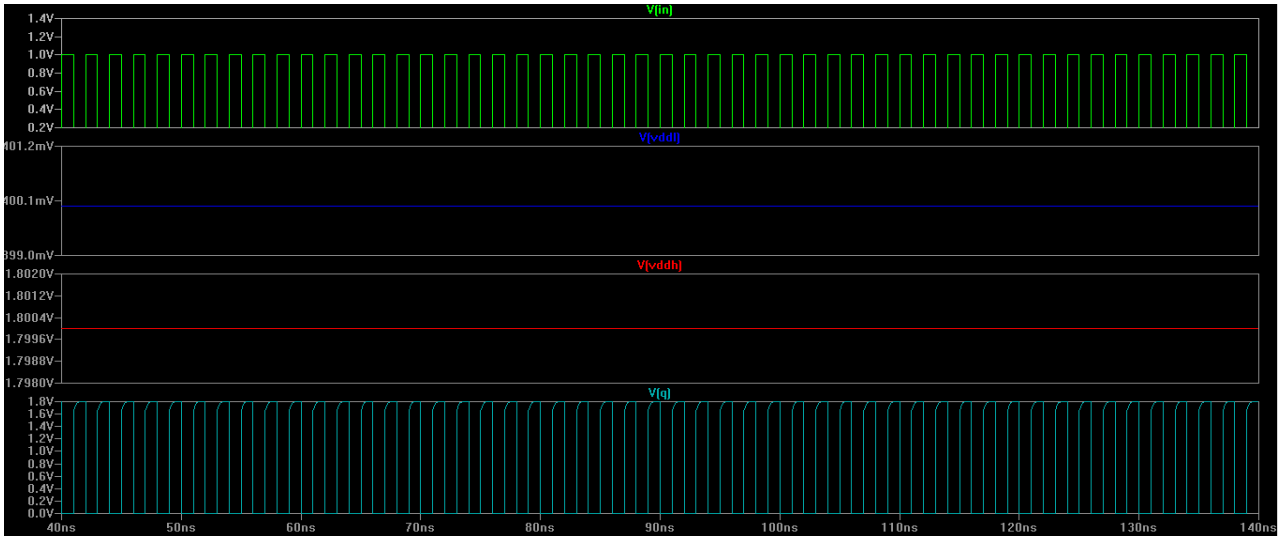

Fig. 4.2.Output waveform of conventional voltage level shifter

SIMULATION RESULTS OF THE PROPOSED CIRCUIT (VDDH = 1.8 V)

Frequency	$V_{DDL,min}$ (V)	Power (μW)	Delay (ns)
5 MHz	0.38	0.98	45
10 MHz	0.41	1.68	24.3
20 MHz	0.44	2.77	13.65
50 MHz	0.49	5.72	5.81
100 MHz	0.54	10.2	2.86
200 MHz	0.6	17.66	1.46
500 MHz	0.72	47	0.63
1 GHz	0.9	95	0.34

In the proposed structure, the typical PVT corner involves typical nMOS and pMOS transistors, a high supply voltage of VDDH = 1.8 V, and a temperature of 25 °C. Moreover, slow-nMOS, fastpMOS, VDDH = 1.8% + 10% = 1.98 V, and a temperature of 0 °C were chosen as the worst corner. This is due to the fact that a larger difference between VDDL and VDDH as well as fast-pMOS and slow-nMOS increase the mentioned contention between the pull-up and the pull-down devices. In addition, in the subthreshold region, a lower temperature results in a smaller current for the devices leading to increase the propagation delay. On the other hand, for the best corner, simulations show that the minimum delay occurred for fastnMOS, fast-pMOS, VDDH = 1.8%–10% = 1.62 V, and a temperature of 120 °C. Fig. 6 shows the simulation results of the delay and the power dissipation of the proposed level shifter versus the value of VDDL, for the typical, worst, and best PVT corners. It can be observed that the circuit works correctly at all the PVT corners for an input frequency of 1 MHz.

To study how the process and temperature variations as well as the mismatch between the devices affect the operation of the proposed circuit, a 1000-point Monte-Carlo simulation has been performed. The normalized standard deviation values (σ /μ) of the delay and power dissipation are 0.56 and 0.32, respectively.

In order to study the main contributor of the static current in the proposed circuit, consider the situation in which the input is "High." Since MN7 is OFF, the gates of MP6 and MP7 are pulled up until the value of VDDH − |Vth|. Therefore, a static subthreshold current (the main contributor of the static current) flows through MP7, MP5, and MN5. It should be noted that as VDDL (the driven voltage of the gates of MP5 and MN5) increases, the drain–source voltage of MP7 is decreased leading to a smaller current in MP7 and therefore a smaller static current.

5. CONCLUSION

In summary, the new inductor-based boosting technique shows promising results for improving Vmin, access time, and power consumption. This novel resonant supply boosting concept was explored through theoretical modeling, simulation, and measured hardware. The 14-nm FinFET SOI test chip measurement results verify simulations, suggesting improvements over the capacitive boosting technique alone. Although this paper provides only an initial investigation into resonant supply boosting, there are numerous avenues to further optimize the proposed technique, which may be beneficial for future low power processors, accelerators, and IoT applications.

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