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Implementation of High Speed Approximate Adder for Effective Area and Low Power

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ABSTRACT

In most digital signal processing (DSP) applications like image processing and speech processing, human beings can collect useful information from slightly inexact outputs. Approximate circuits consume less power, require less number of transistors and have less propagation delay than exact circuits. Approximate adder is the building block of inexact computing for DSP applications. This paper presents a design of a 32-Bit approximate adder which has low power consumption and requires less number of transistors than existing approximate adders. The proposed approximate adder has power savings of 8% for 32 -Bit as compared to existing designs. The proposed adder has significant reduction in area (number of transistors) than existing designs.

Keywords: Digital signal processing, Image processing and Speech processing.

1. INTRODUCTION

The rapid evolution in the field of VLSI has led to portable electronic devices capable of performing complex operations. This has been possible through the use of low-power VLSI design techniques. Inexact Computing is one of the techniques used for low-power VLSI design. The word computing usually refers to the exact results of computations. Inexact computing is the technique of using approximate circuits rather exact circuits to perform the computations. These approximate circuits result in incorrect outputs for some input combinations. This reduces the hardware required for the design of the system as compared to accurate computing. As a result inexact computing offers low power consumption and high speed (less propagation delay) for the system. However, inexact computing is best suitable for DSP applications, such as image, audio and video processing where exact results are not required. This is because the human being, who is the receiver of the results of the computations, cannot perceive the results beyond. This reduces the hardware required for the design of the system as compared to accurate computing. Approximate adders are the building block for any arithmetic circuit used in inexact computing. Approximate adders are derived from accurate adders based on various approximations which have incorrect outputs for sum (S) and carry out (Cout) for some input combinations.

The approximation reduces the number of transistors in adders as compared to accurate adders. Thus approximate adders also decrease power consumption and propagation delay as compared to accurate adders. Various approximate adders have been reported in literature. However approximate adders using CPL suffers from low output voltage swing. Yang proposed transmission gate (TG) based approximate adders which offered good output voltage swing but consumed more power than approximate adders based on CPL . It required a large number of transistors and also increased the power consumption and delay. Nanu *et al*. designed approximate adder using complementary pass transistor logic (CPL) which offer advantage in terms of power and delay. Another XOR/XNOR based approximate adder reported in was derived from ten transistors (10T) accurate adder. This

approximate adder suffered from low output swing as compared to approximate adders based on CPL. Buffers are required to restore the output swing which again increases the power consumption and delay.

The rest of the paper is organized as follows. Section II presents proposed 1-Bit approximate adder. Section III presents the simulation result of 1-Bit .Approximate Adder and comparison with other approximation. Thus approximate adders also decrease power consumption and propagation delay as compared to accurate adders. The approximate adder based on 14T requires offers good output voltage swing and requires less number of transistors than approximate mirror adder design and approximate adders based on TG and CPL. The proposed 1-Bit approximate adder is also compared with existing designs based on total error distance (TED) which measures the accuracy of the circuit adders. Design of 32-Bit approximate adder and comparison with other 32-Bit approximate adders is given in Section IV. Finally Section V concludes the paper.

2. PROPOSED 1-BIT APPROXIMATE ADDER

The approximate adder is derived from accurate adders based on approximations. In this paper, the proposed approximate adder is derived from 14T accurate adder reported in . The 14T accurate and proposed approximate adders are discussed below.

A. Accurate Adder

The accurate mirror adder and accurate adders based on transmission gate (TG) and complementary pass transistor logic (CPL) require large number of transistors [3, 4, 6, 8]. This leads to increase in the area of the circuit. The power consumption and propagation delay are also high. The accurate adder employing ten transistors (10T) suffers from low output voltage swing. Buffers are needed to restore the voltage swing. Use of buffers increases the power consumption, area and propagation delay. In this paper, a 14-transistor (14T) accurate adder has been chosen for implementing the approximate adder. This 14T accurate is based on hybrid CMOS logic style which uses combination of TG and CPL. This 14-transistor accurate adder has good output voltage swing than 10T accurate adder and has low power consumption, less error and propagation delay than accurate mirror adder and accurate adders based on TG and CPL. This 14T accurate adder uses significantly less number of transistors than mirror adder and TG and CPL based adders. The 14T accurate adder is shown in Fig. 1. The accurate adder can be easily approximated using the four approximations explained in next sub-section.

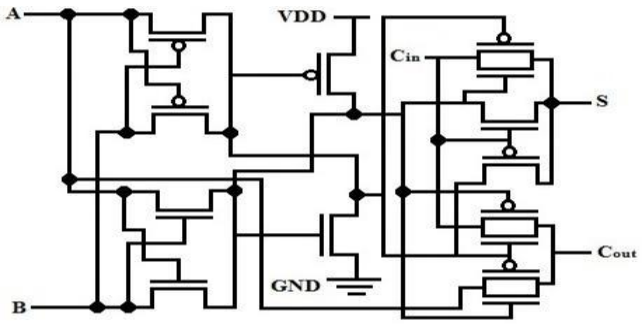


Fig. 1. 14T Accurate Adder

B. Approximate Adder

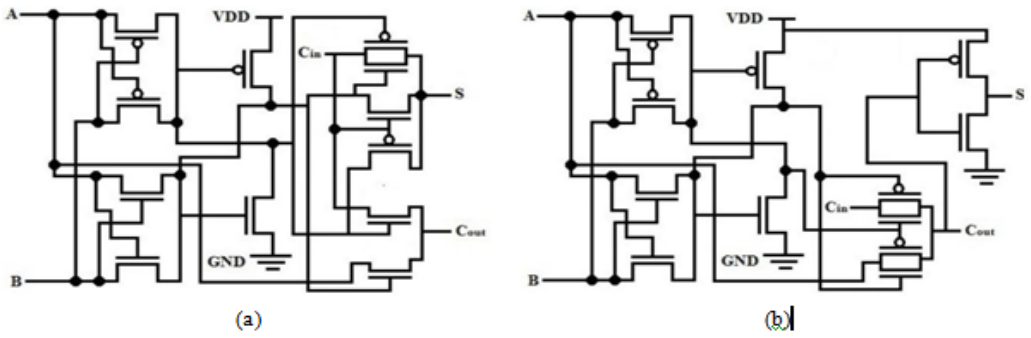
The approximate adder has error in output of sum (S) and carry out (Cout) for some input combinations. This error in output (incorrect output) results because of approximations done on the accurate adder circuits. For these approximate adders, error metrics called error distance (ED) and total error distance(TED) are used to assess the approximated (inexact) results with respect to the correct (exact) results [2].where *i* and *j* are the indices for the bits in *a* and *b*, respectively. The total error distance (TED) is defined as the sum of the EDs for all the inputs of a full adder. The TED is used to assess the effectiveness of the proposed approximate added designs. The proposed approximate adder using 14T are based on following four approximations (Appx.).

1) Approximation 1 (Appx.1): Transistors are removed from the accurate adder wherever possible without creating short-circuits and open-circuits. Also, the outputs resulting from the approximation should not be indeterminate. The circuit diagram of adder based on Appx. 1. The outputs for S and Cout. This approximation produces correct result for all input combinations but reduces only two transistors which is very less. The corresponding error distance is zero as shown in fig 2(a).

2) Approximation 2 (Appx.2): In Appx. 2, the sum (S) is taken as inverted output of carry out (Cout) which results in reduction of two transistors as shown in Fig. 2(b). This approximation gives incorrect output in S for two input combinations as shown in Table I. The cross-mark (X) in output represents incorrect output.

3) Approximation 3 (Appx.3): Appx.3 is the combination of Appx.1 and Appx.2. This approximation produces incorrect outputs in S for two input combinations but it reduces four transistors in the adder circuit. The outputs of the approximate adder based on this approximation as shown in fig 2(c).

4) Approximation 4 (Appx.4): In Appx.4, the output Cout is directly taken from input A. This approximation results in incorrect output in Cout for two input combinations. This results in reduction of four transistors in adder circuit as shown in fig 2(d) .



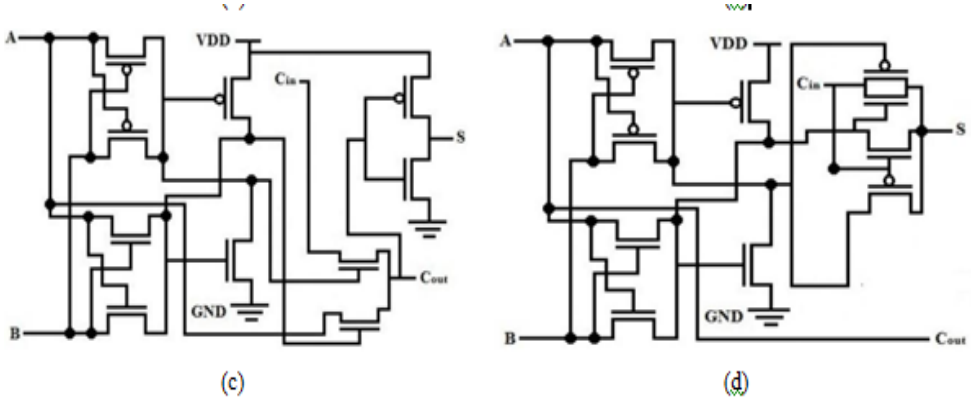


Fig. 2. Approximate Adder based on (a) Appx.1 (b) Appx.2 (c) Appx.3 (d) Appx.4

C. Variable Length CODEC

Stephen Molloy and Rajeev Jain proposed a procedure rang Look table partitioning in a Variable length encoding and decoding design to accomplish low power utilization. Variable length coding is a lossless type of coding which has been viably connected in the MPEG and JPEG image compression models. To accomplish decreased power utilization in mixed media frameworks, low power, high throughput, outlines are required for all means in the pressure and decompression forms including variable length encoding and decoding. The wellspring of force utilization in a variable length encoder and decoder is look-into table which contains the mapping from source images to variable-length codewords. The low power variable length encoder (VLE) engineering is appeared and the low power variable length decoder (VLD) design is appeared.

TABLE I. OUTPUTS FOR ACURATE AND APPROXIMATE ADDERS

Inputs			Accurate Outputs		Approximate Outputs											
					Appx. 1			Appx. 2			Appx. 3			Appx. 4		
A	B	C_{in}	S	C_{out}	S	C_{out}	ED	S	C_{out}	ED	S	C_{out}	ED	S	C_{out}	ED
0	0	0	0	0	0	0	0	1 (X)	0	1	1 (X)	0	1	0	0	0
0	0	1	1	0	1	0	0	1	0	0	1	0	0	1	0	0
0	1	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0
0	1	1	0	1	0	1	0	0	1	0	0	1	0	0	0 (X)	2
1	0	0	1	0	1	0	0	1	0	0	1	0	0	1	1 (X)	2
1	0	1	0	1	0	1	0	0	1	0	0	1	0	0	1	0
1	1	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0
1	1	1	1	1	1	1	0	0 (X)	1	1	0 (X)	1	1	1	1	0

3. SIMULATION RESULTS FOR 1-BIT APPROXIMATE ADDER AND COMPARISON WITH OTHER APPROXIMATE ADDERS

The approximate mirror adder (MA) and approximate adders based on TG and CPL have been obtained using the four approximations (Appx.1-Appx.4) discussed in previous section for uniform comparison with the proposed approximate adder using 14T. All the circuits have been designed in cadence virtuoso tools using 45-nm technology and simulated at 1V power supply. The detailed simulation results are shown in Table II. The total error distance (TED) has also been calculated for all the approximations by evaluating the error distance (ED) for each design in each approximation using equation (1) as shown in Table II.

TABLE II. SIMULATION RESULTS FOR 1-BIT PROPOSED AND EXISTING APPROXIMATE ADDER

Approximations	Approximate Adders	Propagation Delay(ns)	Average Power(μW)	Transistor Counts	Total Error Distance (TED)
Approximation 1 (Appx.1)	MA [3]	0.032	0.047	20	2
	TG [6]	0.050	5.590	20	0
	CPL [8]	0.018	0.040	20	0
	14T [Proposed]	0.029	0.030	12	0
Approximation 2 (Appx.2)	MA [3]	0.043	0.028	14	2
	TGA [6]	0.044	5.590	22	2
	CPL [8]	0.031	0.046	18	2
	14T [Proposed]	0.016	0.033	12	2
Approximation 3 (Appx.3)	MA [3]	0.026	0.028	11	3
	TGA [6]	0.165	5.600	20	2
	CPL [8]	0.337	0.042	14	2
	14T [Proposed]	0.146	0.045	10	2
Approximation 4 (Appx.4)	MA [3]	0.015	0.025	11	3
	TGA [6]	0.038	5.580	18	4
	CPL [8]	0.018	0.029	12	4
	14T [Proposed]	0.009	0.025	10	4

As reported in Table II, the proposed 1-bitapproximateadder using 14T has less power consumption than all other approximate adders in approximations 1 and 4. The proposed approximate adder has the least delay in approximation 2. The transistor counts for proposed approximate adder have reduced as compared to adders of the other three logic styles. The TED for proposed design of approximate adder using 14T is either equal or less than other designs of approximate adders except for Appx.4 where only mirror adder (MA) has a lesser TED.

4. DESIGN OF 32-BIT APPROXIMATE ADDER AND COMPARISON WITH OTHER 32BIT APPROXIMATE ADDERS

The proposed 32-Bit ripple carry approximate adder is designed using eight blocks of 4-Bit ripple carry approximate adder. This 4-Bit ripple carry approximate adder is designed using 1-Bit approximate adders of 14T based on three approximations (Appx.1-3). 1-Bit approximate adder based on Appx.4 is not used because Appx.4 introduces error in Cout which will introduce error in next bit of ripple carry adder if used.

The least significant bits in 4-Bit ripple carry approximate adder is added by 1- Bit approximate adder based on approximation (Appx.1). The next two significant bits are added by 1-Bit approximate adder based on Appx.3 and Appx.2 respectively. The most significant bits are again added by 1-Bit approximate adder based on Appx.1. The least and most significant bits are added by 1- Bit approximate adder based on Appx.1 because Appx.1 does not introduce any error in S or Cout. Thus no error will be introduced in addition of higher bits. The 32-Bit mirror approximate adder (MA) and approximate adders using TG and CPL have been implemented like the proposed 32-bit approximate adder. The 32-Bit adder based on 1-Bit approximate Mirror adders requires 16 additional inverters.

The circuits of 32- Bit proposed and other existing approximate adders have been designed in Cadence Virtuoso tool using 45-nm technology and simulated at 1V power supply. The simulation results based on some samples are shown in Table III. The maximum delay among all outputs was considered. The power consumption and transistor

counts for the proposed 32- Bit approximate adder have reduced as compared to 32-Bit mirror approximate adder and 32-Bit approximate adders based on TG and CPL.

TABLE III. SIMULATION RESULTS FOR 32-BIT PROPOSED AND EXISTING APPROXIMATE ADDER

Approximate Adders	Propagation Delay(ns)	Average Power(µW)	Transistor Counts
MA [3]	0.070	1.51	552
TG [6]	0.150	179.50	656
CPL [8]	2.895	3.02	576
14T [Proposed]	0.222	1.39	368

5. CONCLUSION

This paper presents an approximate adder derived from 14T accurate adder. The proposed approximate adder consumes low power than mirror approximate adder and approximate adders based on TG and CPL. The number of transistors for proposed approximate adder is much less than other approximate adders. The proposed as well as existing approximate adders were also compared based on total error distance (TED). Even though some outputs were incorrect due to approximations, it will have very little impact on the performance of the circuits when applied for DSP applications where incorrect results are acceptable. This paper also presents a design of 32-Bit approximate adder and compares it with other similar existing designs. These approximate adders are very useful for arithmetic circuits used in DSP applications and other applications where inexact computing is used.

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