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Technological Boom of Multi-Patterning

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ABSTRACT

Multi-patterning technology was started with the 20 nm node to reduce lithographic limitations in current IC manufacturing processes. While processes like double and triple patterning may sometimes seem like magic, successfully implementing multi-patterning compliance in the IC design and verification flow requires a thorough understanding of multi-patterning techniques and their impact on your design. Learn what multi-patterning is, why you need it, and how Caliber Multi-Patterning software can help you effectively and efficiently incorporate multi-patterning into your leading-edge designs.

Keywords: Double patterning, Triple patterning, Multipatterning, 22nm, 16nm, 14nm, 10nm, 7nm, Lithography and LELE.

1. INTRODUCTION

Multi-patterning (MP) is one of the latest in a long line of technological magic tricks that have enabled the IC industry to continue producing leading-edge chip designs in the absence of next-generation lithography technology (Figure 1). The introduction of MP technology gave us the capability to successfully image designs at 20 nm and below. However, while the actual MP process occurs in the foundry, some MP solutions impose new layout, physical verification, and debug requirements on the design side. Designers must purchase MP software, and do additional work in the design layout and verification. MP decomposition and checking capabilities require a new software engine to properly analyze layouts. MP violations can be extremely challenging to debug, and fixing them is mandatory, not just recommended. Moreover, MP's potential impact on capacitance and parasitic must be accounted for. In this paper, we'll explain the basics of Multi-patterning techniques, and discuss how they affect different aspects of the design and verification flow.

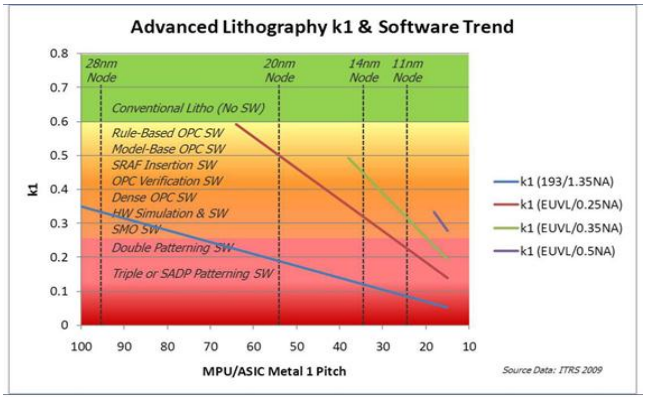

Figure 1: Advance lithography k1 and software trend

2. MULTI-PATTERNING TECHNIQUES

While not all MP techniques are implemented in the design flow, it is useful to understand the many implementations of MP that are emerging, and the differences in their application

2.1 LELE DP

On the design side, "double patterning" (DP) almost always refers to the Litho-Etch-Litho-Etch (LELE) pitch-splitting process. The active, contact, via, and lower metal layers began using LELE DP at 20 nm node. The LELE DP technique requires dense layouts that can't be printed with a single exposure to be split into two lower-density layout masks. The foundry then uses two separate exposure processes to form two coarser patterns, which are superimposed to form a single finer image on the actual wafer.

Color (mask) assignments in LELE DP are based on spacing requirements. Polygons that are closer than the minimum DP spacing must be assigned to different masks. Figure 2 shows how MP is used to split (decompose) the original drawn layout into two new layers, either automatically by a specialized MP tool like Calibre Multi-Patterning, or manually by the designer.

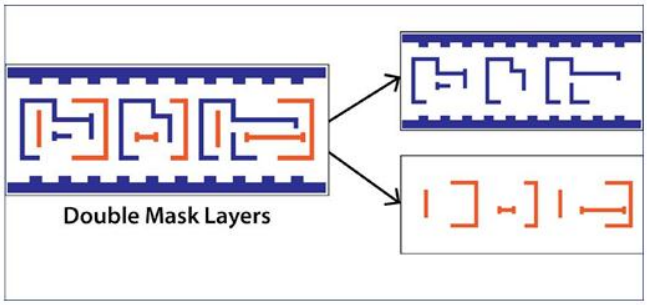

Figure 2: LELE DP layout decomposition

2.2 LINE/CUT DP MASKS

The line/cut DP process is "hidden" from the design side. The poly (gate) layer in the 20 nm process node can only contain uni-directional lines, which create the first "line" mask. A second "cut" mask creates the gaps (spaces) in these lines (Figure 3). Designers do not draw these two masks or perform decomposition checks for this process. The

restrictive design rules of the poly layer ensure that the generation of these two masks is possible.

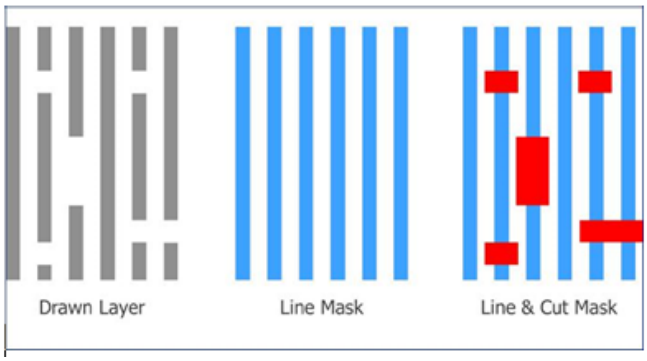

Figure 3: Line/Cut two-mask decomposition

2.3 LELELE TP

The 10 nm node introduced two new variations of MP. The first is LELELE pitch-split triple patterning (TP), which requires decomposition of the original layer into three masks (Figure 4). Just like LELE DP, the shapes from the three masks are combined during manufacturing to create the final shapes. The LELELE TP process is used for layers like contacts, re-distribution interconnect, and/or M1.

Because this process is so similar to the 20/16/14 nm DP process designers may assume the transition to LELELE TP is simple. However, there are some important differences that introduce new challenges to the designer, foundry, and EDA tools.

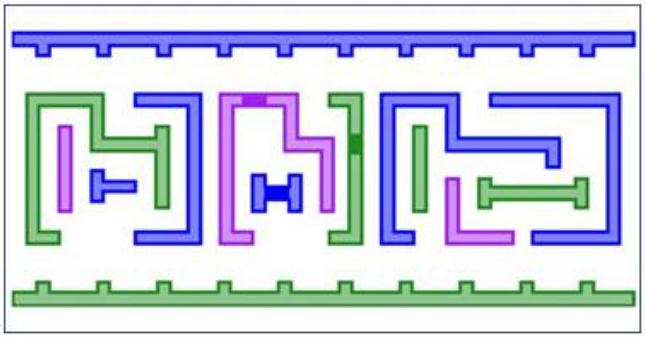

Figure 4: LELELE TP decomposition

3. UNDERSTANDING MP COLOR CONTROL

LELE DP provides four possible LELE DP design flows (Figure 5). The first three flows are two-color flows, in which the designer tapes out two separate "color" layers for any layer that will be double-patterned. The fourth flow is the "colorless" flow, in which the designer only tapes out a single layer and the foundry performs the decomposition.

The difference between the first three flows is the level of automation used to create the two layers. In manual decomposition, the designer decides how to implement the design in two masks, draws both mask layers by hand, and checks for MP compliance with traditional design rule checking (DRC) tools. However, decomposing layouts by hand is very time-consuming and difficult, and on a large block, impractical. For these reasons, manual decomposition is rarely used.

In automated decomposition, the designer draws a single layer, and then uses a dedicated MP tool like Calibre Multi-Patterning to automatically decompose the layer and check for MP compliance. Specialized MP checks in Calibre Multi-Patterning help the designer better understand the complete set of polygon interactions causing decomposition errors.

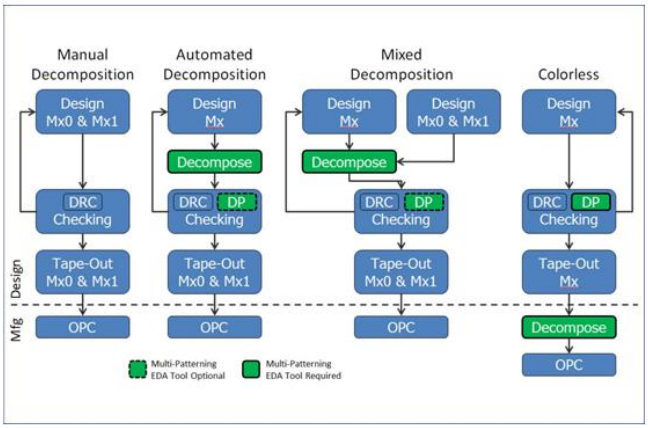

Figure 5: Flow charts of the various DP decomposition methodologies

In automated decomposition, the designer draws a single layer, and then uses a dedicated MP tool like Calibre Multi-Patterning to automatically decompose the layer and check for MP compliance. Specialized MP checks in Calibre Multi-Patterning help the designer better understand the complete set of polygon interactions causing decomposition errors.

With mixed decomposition, the designer performs some decomposition manually, and then uses the Calibre Multi-Patterning tool to automatically decompose the remaining shapes and check the entire design. Mixed decomposition is commonly used when designers incorporate previously-decomposed cells into a new layout that is still in one layer.

In the colorless flow, the designer draws only a single layer, relying on the specialized MP checks to identify locations that cannot be correctly decomposed. The single layer must be modified until these checks are clean. The foundry decomposes the layout into two layers after tapeout.

Choosing an MP flow is all about trade-offs. Manual decomposition gives the designer the most control over the final result. Using a colorless flow employs a traditional design style, but means handing over control of the decomposition to the foundry. Your choice of foundry may also limit your options. Both major foundry eco-systems support the colorless flow, but only one allows the designer to tape out the two masks. We suggest you hold conversations with your foundry and EDA vendor to understand which flows are supported and what tool capabilities exist.

4. ANCHORING AND SEEDING

Even in a mixed or colorless flow, a designer may need to control some of the coloring. For example, the parasitic impact of misalignments associated with LELE DP can

usually be accounted for without specific coloring information (particularly in the digital design areas). However, very critical circuits, nets, or cells may require designer control of the coloring to reduce potential randomness in variability that can occur if the foundry arbitrarily colors them. Mixed decomposition lets the designer control the coloring of part of the layout, while ensuring the uncolored portion has at least one valid coloring solution for the foundry to apply after tape out.

The designer can "anchor" a single layer shape by overlaying a marker layer that tells Calibre Multi-Patterning to assign the shape to a particular mask. This anchor also influences the allowed coloring of neighboring shapes within the separator distance, which reduces the number of coloring options.

In a similar technique called seeding, the designer also draws a marker layer to specify the mask color, but this marker does not cover the entire original polygon. Calibre Multi-Patterning uses this "seed" marker to set the coloring for the rest of that shape (Figure 6).

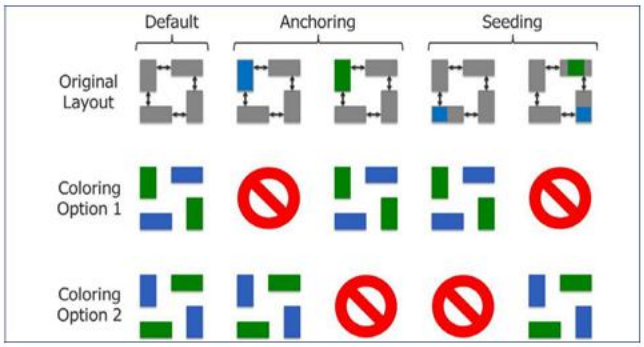

Figure 6: Anchor and speed markers, and the resulting valid coloring solutions

Anchoring and seeding enable a nice tradeoff between providing designers control of coloring where they need it, and ensuring manufacturing flexibility to arbitrarily color the rest of the layout as desired. However, this capability also introduces new types of DRC violations that must be checked before tapeout.

5. DEBUGGING MP ERRORS

Debugging MP errors is probably the most challenging aspect of MP implementation. There are three LELE DP errors that are similar to traditional minimum spacing DRC errors:

- A minimum opposite mask spacing violation occurs when two polygons are so closely spaced that they cannot be manufactured even if they are placed on opposite masks.
- A self-conflict violation occurs when a single polygon has a notch space less than the minimum opposite mask spacing constraint. The spacing cannot be resolved by alternating mask assignment because it only involves a single polygon that must be on one mask or the other.
- An anchor self-conflict violation occurs when a single polygon has two or more different anchor/seed markers placed on it. Since the polygon has to be assigned to a single mask, both mask anchoring requests cannot be honored simultaneously.

In addition to these errors, there are two complex LELE DP errors:

- An odd cycle violation identifies a group of polygons spaced such that any neighboring polygons must have opposite colors, but because of the odd number of polygons in the cycle, this color alternation cannot be evenly divided by two colors.
- An anchor/seed path violation occurs when a designer anchors/seeds a pair of polygons to ensure they are placed on certain mask layers, but there is a series of interacting polygons (path) between the two anchors/seeds that cannot be colored in alternating colors that align with the anchor/seed colors.

Figure 7 shows these complex errors. The red conflict rings indicate two odd cycle violations. The dark purple anchor path shows a color alternation violation between the anchored polygon at the top and the anchored polygon at the bottom of the cell.

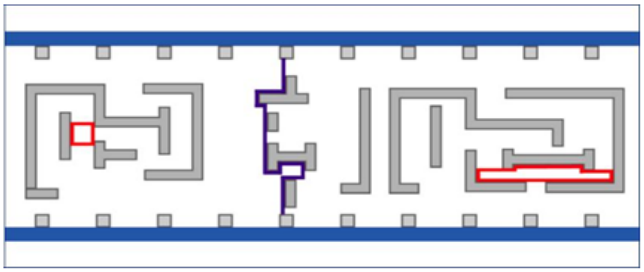

Figure 7: Odd cyle and anchor path errors

Unlike traditional DRC errors, these complex MP errors usually have multiple solutions. Since both error types result from the interaction of multiple polygons simultaneously, fixing any single interaction in the set can fix the error. For instance, if an odd cycle error contains three polygons with three spacing interactions, editing any single polygon or spacing can fix the entire set. However, some fixes can create new MP violations.

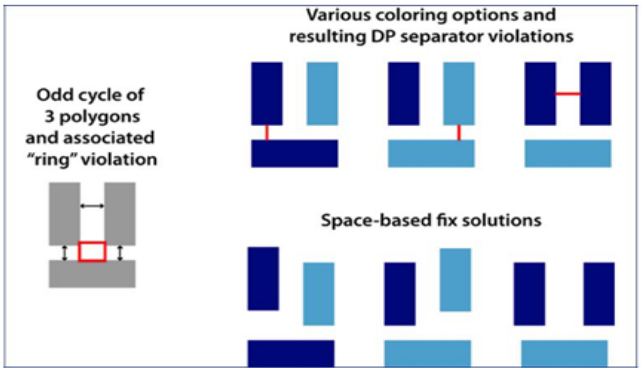

Figure 8: Odd cycle MP error and potential space-based fix options

6. CUTS AND STITCHES

Using coloring, the only way to fix an odd cycle violation is to increase the spacing between any two of the polygon pairs (Figure 8). Of course, adding space can cause ripple effects with other layers, generate additional MP errors, and may ultimately increase the size of your layout.

To fix odd cycle violations without adding space, designers can cut (divide) a polygon, and assign different colors to each section (Figure 9).

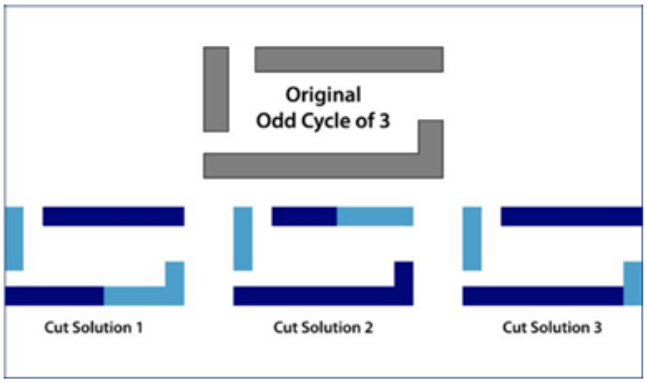

Figure 9: Cuts can change an odd cycle into an even cycle

However, cuts can cause manufacturing problems [2]. Even with advanced OPC techniques, lithographic "rounding" of line ends can cause additional resistance in an overlap, or create an open. To allow for lithographic rounding and misalignment, designers must stitch (overlap) the polygons at the cut location (Figure 10).

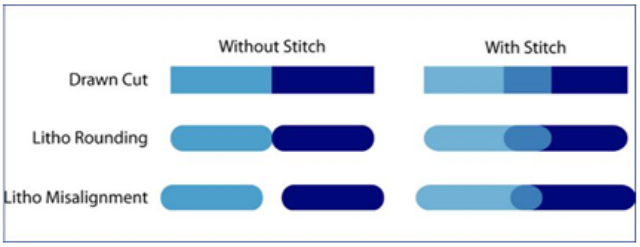

Figure 10: Lithographic effects require stitches

A stitch can introduce new DRC violations, depending on where it is used. Figure 11 shows how DRC constraints help limit the candidate locations for legal stitches.

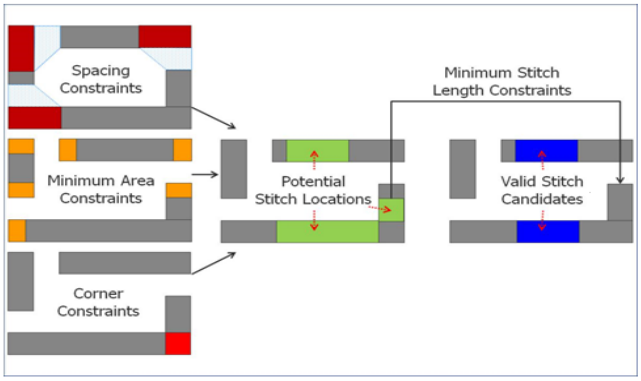

Figure 11: DRC constraints limit the placement of legal cuts and stitches in a layout

Some foundries support the use of cuts/stitches in MP design, with the goal of providing design density and error minimization, while other foundries have decided not to support cuts/stitches to minimize complexity of design and manufacturing. If your foundry allows cuts and stitches, the automated cut and stitch functionality in Calibre Multi-Patterning uses specialized rule decks to provide fully MP-compliant designs.

7. DEBUG ORDER MATTERS

Another critical aspect of MP errors is understanding the optimal fix order. Many MP error types interact with and affect the results of the others. Designers should always observe the following fix order:

1. All minimum opposite mask spacing violations,
2. Self-conflict violations,
3. Anchor self-conflict violations,
4. Odd cycle errors,
5. Anchor/seed path errors.

8. MP-AWARE PLACEMENT-FRIENDLY CELL DESIGN

Cell libraries designed for processes that don't require MP layers are usually placement-independent. This independence allows the cells to be very compact, while providing maximum flexibility for the place and route (P&R) tools to minimize area utilization. With MP, placement independence can no longer be taken for granted, even when each cell is MP-clean.

Figure 12 shows how an MP error can occur on a single interconnect layer when two MP-clean standard cells are placed together. Because of this MP restriction, these two cells cannot be placed directly next to each other. Adding extra space can eliminate that odd cycle, but it increases the design area and still doesn't guarantee placement independence. In Figure 13, because the interior polygons interact at minimum spacing with the power and ground polygons, an odd cycle is formed that traverses through the power and ground rails. Adding height to the cells eliminates these odd cycles, but further increases design area.

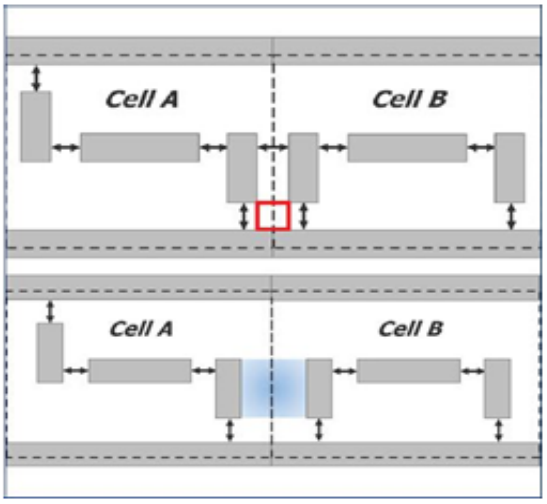

Figure 12: Two MP-clean cells can form an odd cycle error when placed next to each other

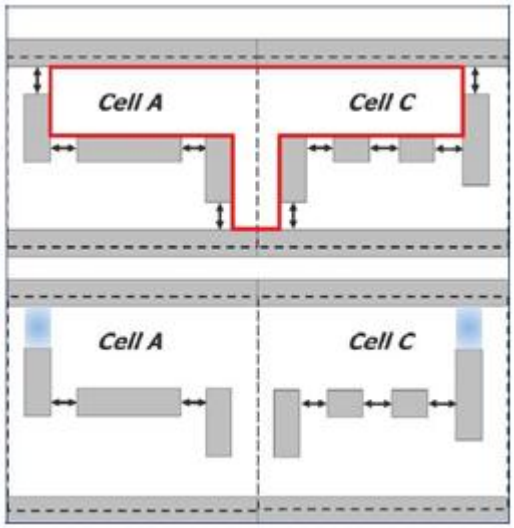

Figure 13: Increasing height can avoid MP odd cycles, but increases design area

9. MP ROUTING CONSIDERATIONS

MP methodologies at the cell level must be aligned with MP methodologies at the routing level to ensure optimal results. Understanding how automatic routing is affected by MP begins with the interaction between decisions made at the cell design level and decisions made at the routing level. For instance, if you allow the router to make connections from pin to pin between cells on the same metal layer on which the pins reside, the methodology that determines constraints on pin coloring during cell development must be reviewed for MP compatibility.

Pin coloring in the cell can be affected two ways. If the pin polygons are "pre-colored" or "anchored," their color is constrained. If pin colors are not pre-determined, spacing interactions with other polygons in the cell may define color differences between pins. Spacing interactions within the cells can force certain color differences between various pins in various cells (Figure 14). These forced color differences may constrain cell-to-cell routing.

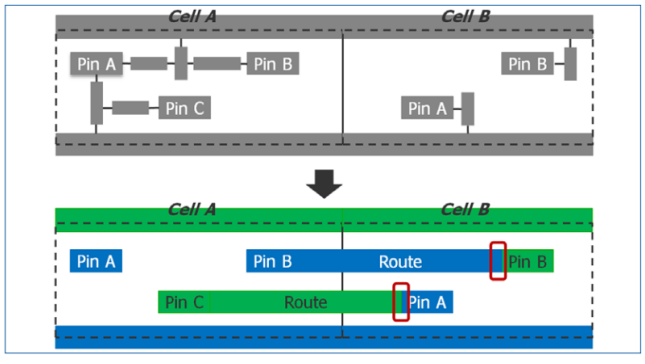

Figure 14: Cell-to-cell routing limitations due to forced color differences on cell pins

When dealing with auto-routed layers, it is important to remember that MP odd cycle violations can involve hundreds or thousands of polygons, and extend across the full chip. Figure 15 shows both local and long-range cycle violations in a routed layout.

In addition, MP violations can have multiple solutions. The compute processing needed to find and fix such long-range potential MP violations is counter to the goal of high-speed automated routing. Routers do include MP checking in their engines, but you should adjust your expectations regarding both runtime impact and the ability to find unresolved errors in post P&R verification runs.

Luckily, encoding MP checking into the router tech file is not the only technique available to help automated routing produce MP-compliant layouts. Advanced automated routing tools like Mentor Olympus-SoC now incorporate MP prevention and repair techniques to reduce the possibility of creating an MP odd cycle violation:

- No off-track routing
- No odd jogs
- Increased tip-to-tip spacing
- Increased spacing to non-preferred or fat wires

These rules are easily enforced and reduce the possibility that a MP odd cycle violation will be created. However, extensive use of such rules constrains the flexibility of the routing solution, can force an increased use of vias and extra routing tracks on other layers, and may increase the chip area. These changes can increase yield sensitivity and, potentially, die area.

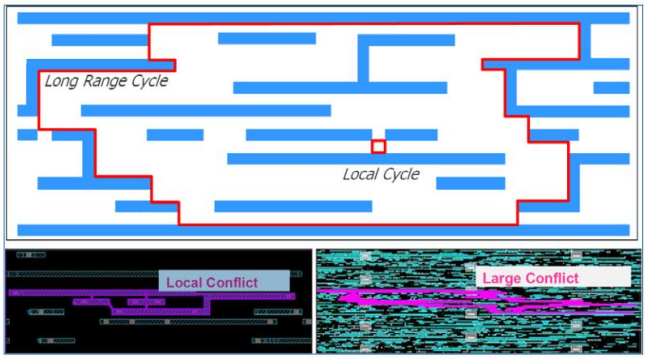

Figure 15: Local and long-range odd cycle violations in routed layout

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Also, restricted routing does not guarantee complete avoidance of MP violations. A full production verification engine like Calibre must be run on the routed layout to catch violations the routing engine didn't detect. To make that easy, Calibre has integrations with all the major routers, and in-memory integration with Olympus-SoC (using Calibre InRoute).

However, while Calibre can ensure that all MP violations are found, the challenge for the routers is fixing the detected errors. Typically, the router performs a re-route within a

"halo" (expanded area) around the error marker, and then re-checks the changes in the halo to ensure new errors were not introduced. In Figure 16, the original odd cycle is relatively localized, and the error appears to be corrected successfully if only the halo region is re-checked. However, a new cycle violation was introduced that extends far beyond the original halo region.

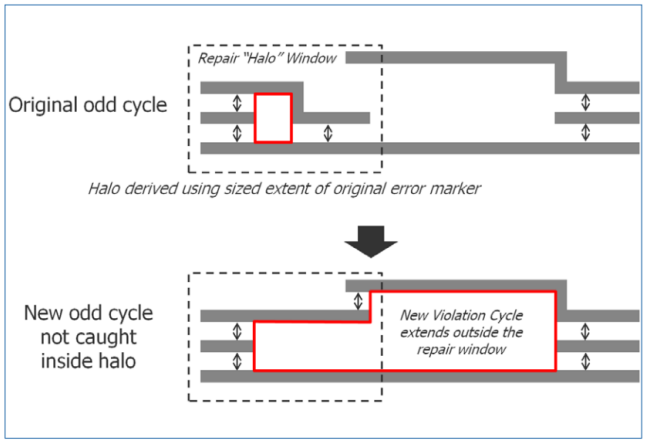

Figure 16: MP odd cycle errorrepair and missed new odd cycle error using a traditional halo region

Extending the halo region doesn't help, because there may always be a new odd cycle error outside the halo. There is no halo definition that guarantees validation of a routing DP fix unless it extends to cover the whole chip.

An alternative method arbitrarily assigns coloring during the checking pass, then carries these colors into the halo fix and re-validation to see if the newly moved polygons generate a same-color spacing violation. However, arbitrary color assignment can lead to false MP errors, and severely restricts the MP solution space.

In the end, MP-aware and MP-compliant automated routing is no easy task, but you can be successful. Advanced routers like Olympus-SoC do a very good job of utilizing integrated MP checking, restrictive routing rules, and automated fixing of Calibre errors to obtain the best result possible with reasonable run times. However, you should expect some iteration using a sign-off verification tool like Calibre. You also must align your cell design methodology with your routing methodology in regards to MP.

10. SUMMARY

Multi-patterning is not magic. It is a complex new technique of IC manufacturing that requires new approaches to design and verification, and new knowledge and preparation on the part of companies and designers. Tools like Calibre Multi-Patterning can help designers implement multi-patterning design with confidence, but the more you learn, experiment, and prepare, the better off you will be.

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