Asian Journal of Applied Science and Technology (AJAST)
Volume 1, Issue 7, Pages 76-79, August 2017

Pipelined Direct Mapping Method based Low Power VLSI Architecture for the 4-Tap Wavelet Filter

T.Kalavathi Devi[1] and P.Sakthivel[2]

[1]*Department of EIE, Kongu Engineering College, Tamilnadu, India. Email: kalavathidevi@gmail.com*
[2]*Department of EEE, Velalar College of Engineering and Technology, Tamilnadu, India. Email: sakthi.dpt@gmail.com*

Article Received: 24 July 2017 *Article Accepted: 08 August 2017* *Article Published: 10 August 2017*

ABSTRACT

This paper presents an area efficient and simple design of multidimensional (2D) Daubechies wavelet transform 4-tap (Daub4) with pipelined direct mapping method for image compression. Due to separability property of the multi-dimensional Daubechies, the architecture has been implemented using a cascade of two *N*-point one-dimensional (1-D) Daub4 and Daub6.The 2-dimensinal discrete wavelet transform lifting scheme algorithm has been implemented using MATLAB program for both modules forward daubechies wavelet transform (FDWT) and inverse daubechies wavelet transform (IDWT) to determine the peak signal to noise ratio (PSNR) and correlation in between retrieved image and input image. The architectures were synthesized by VHDL and implemented on Altera®Cyclone II (EP2C35F672C6) Field Programmable Gate Array (FPGA). Experimental results and an analysis of the power consumption, maximum frequency and latency are discussed in this paper.

Keywords: Daubechies Wavelet Filter, Pipelined direct mapping method and MATLAB.

1. INTRODUCTION

Real-time two dimensional (2D) medical image processing is a niche area concerned with the processing of real-time sequences of medical image data which represents a developing trend in medical industries. With a more realistic manner of an atomic structure representation including the information about position, size, shape, and ease of visualization, 2D images provide more accurate parameters for the assessment of pathological changes [1], and thus leading to great advantages for image based screening, diagnosis and treatments.

A particular class of DWT is Daubechies wavelets with taps [2]. They are well-suited and commonly used in image compression applications [3-6]. Here in we refer to the Daubechies wavelets generated from 4 tap filter banks as Daub-4. In particular, whereas the Daub-4 wavelets are often employed in applications where the signals are smooth and slowly varying, for signals bearing abrupt changes, having high undesired noise levels and spikes [7]. Daub-4 wavelets can be highly localized to smooth [8-9] and Daub-6 wavelets have applications in medical imaging, such as the wireless capsule endoscopy where images of fine details are regarded important.

The aim of this paper is to develop an efficient reconfigurable architecture for Daubechies wavelet transform using pipelined direct mapping. Finally, this research is expected to propose a novel architecture of 2-D DWT using various wavelet filters and different design strategies that can be further applied as an intellectual property core for compression systems specifically in telemedicine applications.

The rest of the paper is organized as follows. Section II describes an overview of the issue of matrix transform algorithm. An overview of the related work is given in Section III. Section IV explains the mathematical background for Daubechies wavelet filter. Section V discusses the resulting outcomes. Finally, concluding remarks and further potential ideas to be explored are given in Section VI.

2. CONTRIBUTIONS

2.1 The Problem of complexity for the matrix transform algorithm

The application of 2D real-time image processing uses several building blocks. Its algorithm is computationally intensive algorithm to perform matrix transformation operations. Massive amount of data to be processed have resulted in vast challenges from a hardware implementation point of view.

Computational complexity for the matrix transform algorithms is in the order from O ($N \times \log N$) for FFT to O ($N2 \times J$) for the curve let transform (where N is the transform size and J is the maximum transform resolution level) are computationally intensive for large size problems. For that reason, efficient implementations for these operations are of interest not only because matrix transforms are important, but because they automatically lead to efficient solutions to deal with massive medical volumes.

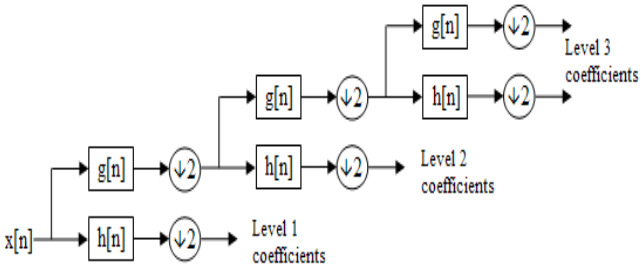


Fig.1.Three-level decomposition of wavelet algorithm

2.2 Prior Art on transpose-Based DWT

Since the aim of this research is on the implementation of 2-D image processing application using MATLAB. The proposed

scalable architecture is based on pipelined direct mapping techniques and it works in two different modes to reduce computational complexity.

3. RELATED WORK

In this section, existing 2D DWT architecture has been designed using MATLAB and VHDL.

3.1 2D DWT

Despite its complexity, there has been an interest in 2D DWT implementation on various platforms. However, a survey of existing literature indicates that the research is still in its infancy as demonstrated by the limited contributions proposed and it can be classified into three categories: architecture development [(10), (11)], Image accuracy, area and power requirement. Since the aim and contribution of this paper is on the implementation of DWT architecture using MATLAB and VHDL environment.

Moreover, the proposed architecture also is low power and can run at higher frequency which fully utilizes the advantages of parallelism and pipelined structures for filter design.

4. MATHEMATICAL BACKGROUND

The Daubechies wavelet transform is defined in essentially the same way as the Haar wavelet transform. The difference between them is the way that the scaling signals and wavelets are defined [(12)]. Interestingly, Daubechies wavelet transform has properties of longer supports for the scaling signals and wavelets. Thus, the Daubechies 4-tap (Daub4) has been used in this study besides it is the most popular choice in medical imaging applications.

***4.1 2D Daubechies 4-Tap Algorithm*:** The Daub4 wavelet is the simplest wavelet among the Daubechies wavelet families. Generally, Daub4 have four scaling signals and wavelets coefficients as given in equation (1) and (2) respectively.

$$h_0 = \frac{1+\sqrt{3}}{4\sqrt{2}}, h_1 = \frac{3+\sqrt{3}}{4\sqrt{2}}, h_2 = \frac{3-\sqrt{3}}{4\sqrt{2}}, h_3 = \frac{1-\sqrt{3}}{4\sqrt{2}} \quad (1)$$

$$g_0 = h_3, g_1 = -h_2, g_2 = h_1, g_3 = -h_0 \quad (2)$$

The 1-level Daub4 scaling signals and wavelet coefficients are defined in matrix form shown in equation (3).

$$\begin{bmatrix} h_0 & h_1 & h_2 & h_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & h_0 & h_1 & h_2 & h_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & h_0 & h_1 & h_2 & h_3 \\ h_2 & h_3 & 0 & 0 & 0 & 0 & h_0 & h_1 \\ g_2 & g_3 & 0 & 0 & 0 & 0 & g_0 & g_1 \\ g_0 & g_1 & g_2 & g_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & g_0 & g_1 & g_2 & g_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & g_0 & g_1 & g_2 & g_3 \end{bmatrix} \quad (3)$$

The wavelet functions are calculated by taking the inner product of the coefficients and data input values. The process of Daubechies wavelet using both scaling and wavelet functions and given as follows.

Step 1: Consider the first row of a set of matrix values in input image:

f =(f (0), f (1), f (2), f (3), f (4), f (5), f (6), f (7))

Step 2: Apply the low and high pass filters along the vector *f*.

$$\begin{bmatrix} h(0)f(0)+h(1)f(1)+h(2)f(2)+h(3)f(3) \\ h(0)f(2)+h(1)f(3)+h(2)f(4)+h(3)f(5) \\ h(0)f(4)+h(1)f(5)+h(2)f(6)+h(3)f(7) \\ h(2)f(0)+h(3)f(1)+h(0)f(6)+h(1)f(7) \\ g(2)f(0)+g(3)f(1)+g(0)f(6)+g(1)f(7) \\ g(0)f(0)+g(1)f(1)+g(2)f(2)+g(3)f(3) \\ g(0)f(2)+g(1)f(3)+g(2)f(4)+g(3)f(5) \\ g(0)f(4)+g(1)f(5)+g(2)f(6)+g(3)f(7) \end{bmatrix}$$

f_1= (5.775,12.439,6.371,0.154,0.961,0.867,-3.121,-0.837)

Step 3: Keep the last half of the vector f_1 fixed while applying low and high pass filter along the first half of the vector.

f_1 =(f_1(0), f_1(1), f_1(2), f_1(3), f_1(4), f_1(5), f_1(6), f_1(7))

Step 4: Apply the low and high pass filters along the first four elements of the vector in f_1.

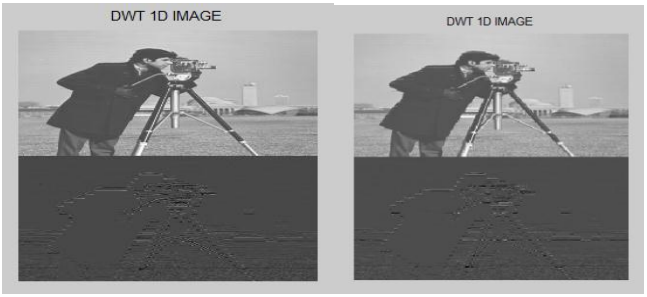
$$\begin{bmatrix} h(0)f(0)+h(1)f(1)+h(2)f(2)+h(3)f(3) \\ h(0)f(2)+h(1)f(3)+h(2)f(0)+h(3)f(1) \\ g(0)f(0)+g(1)f(1)+g(2)f(2)+g(3)f(3) \\ g(0)f(2)+g(1)f(3)+g(2)f(0)+g(3)f(1) \\ f_1(4) \\ f_1(5) \\ f_1(6) \\ f_1(7) \end{bmatrix}$$

f_2 =(223.828,220.482,1.641,-1.327,1.641,1.796,1.443, -2.128)

f_2 values indicate 2D Daub4 wavelet filter compressed values for first row of input image. Likewise, this concept is applied to the full input image for compressed 2D image.

5. RESULTS AND ANALYSIS

MATLAB environment is used to writing appropriate code to simulate the 2D Daub wavelet filter.(FDWT) output shown in Fig.5.Where, (a).4Tap 1D output image, (b).6Tap 1D output image. With (FDWT) MATLAB program the cameraman picture of size (256×256) is used as original input image, it is analyzed for two levels of decomposition, and then the (IDWT) is used to reconstruct the retrieved image from the second level, as shown in the Fig.5.



(a) (b)

Fig.4. 2D Output Image (a).4Tap 1D output image, (b).6Tap 1D output image

To evaluate the performance of proposed architecture, there parameters have been selected including the PSNR, correlation,SIM[. To analyze visually the proposed architectures, both original and reverse process image are given in Fig.6 (a) and (b). The output image uses a gradient color scheme in which the color becomes darker as the utilization of a resource increases. Effectively, it can be clearly seen that the Daub4 implementation requires less complicated mapping in comparison with reverse process image of Daub4.

(a) (b)
Fig.5. (a).Original image, (b).Retrieved image

Table 1.Performance Statistics

IMAGE METRICS	DAUB4	
	1D	2D
PSNR	64.12	69.89
Correlation	.851	.874
Similarity	.901	.962

From the Table 1, it is analyzed that the PSNR, correlation and similarity of the proposed method better results for 2D daub wavelet filter. On the other side, the delivery time taken for a packet of data become the first available output data in the pipelined system.

On the other side, the output waveform of 2D DWT by VHDL using the pipeline system illustrated in Fig. 4. The architectures were synthesized using VHDL and implemented on Altera®Cyclone II (EP2C35F672C6) field programmable gate array (FPGA).

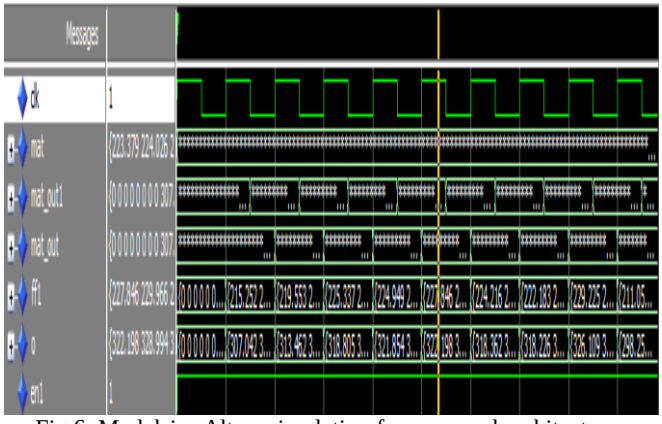


Fig.6. Modelsim-Altera simulation for proposed architecture. Dau4 2D

Altera® Quartus II design flow[19]-[21]has been used as a design flow reference and the proposed two architectures have been implemented on the Cyclone II(EP2C35F672C6). To evaluate the performance of the proposed architectures, three parameters have been selected including the maximum frequency (MHz), power consumption (mW) and latency (ns).

Table 2.Resources Utilization and Overall Proposed Architectures Performance on EP2C35F672C6

Parameters.	Daub4
Latency(ns)	86
Power consumption(mW)	110.64
Maximum frequency(MHz)	19.98

5.2 Discussions

Concerning the higher vanishing moments of Daub6 [13], the implementation of 3-D Daub4 on Altera®Cyclone II (EP2C35F672C6) FPGA yielding 0.43% better maximum frequency and consumes less power by 22.95% . Altera® Quartus II PowerPlay Power Analysis tools are used for the purpose of power consumption estimation by read the verilog value change dump file (.vcd) and derives the toggle rate and static probability data. This .vcd file is created using ModelSim-Altera after the designs are synthesised and fitted to the target device. Analysis for the performance achieved in terms of, maximum frequency, power consumption and latency have reveals that with Daub6, complex designs can be implemented on FPGA and hence carry out a better performance achievements.

6. CONCLUSION

Architecture of 2-D Daub4 wavelet have been proposed in this paper based on pipelined direct mapping method. 1D Daub6 provides better PSNR and correlation values are 69.89 and 0.874 compared with Daub4. Experimentally, the results are verified with PSNR and Correlation. These values are indicates that the proposed Daub4 performance is better. Also, design and FPGA implementation of 3-D Daub4 and Daub6 using other wavelet filters such as Symlet, Coiflet and Biorthogonal as well as various transform size and real 2-D medical imaging modalities will be further explored to demonstrate the efficiency of the proposed architecture in medical imaging compression systems.

REFERENCES

[1] K. A. Wahid, V. S. Dimitrov, G. A. Jullien, and W. Badawy: “An algebraic integer based encoding scheme for implementing Daubechies discrete wavelet transforms”, in *Proc. Asilomar Conf. Signals, Syst. Comp.,* Vol.1, No.109, pp.967–97, 2002.

[2] K. A.Wahid, V. S. Dimitrov, G. A. Jullien, and W. Badawy: “An analysis of Daubechies discrete wavelet transform based on algebraic integer encoding scheme”, *in Proc. 3rd Int. Workshop Digital Computational Video DCV* 2002, pp. 27–34, 2002.

[3] D.-Z. Tian, M.-H. Ha: ”Applications of wavelet transform in medical image processing”, *in Proceedings of International Conference on Machine Learning and Cybernetics, Baoding, China,* Vol.3, No.214, pp.1816–1821, 2004.

[4] M. A. Islam and K. A. Wahid: “Area- and power-efficient design of Daubechies wavelet transforms using folded AIQ mapping”, *IEEE Trans. Circuits Syst. II, Exp. Briefs,* Vol.57, No.9, pp.716–720, Sep. 2010.

[5] M. Jiang and D. Crookes: “Area-efficient high-speed 3D DWT processor architecture”, *IEEE Electronics Letter,* Vol.43, No.53, pp.502-503, 2007.

[6] S. Gnavi, B. Penna, M. Grangetto, E. Magli, and G. Olmo: "DSP performance comparison between lifting and filter banks for image coding", *in Proc. IEEE Int. Acoustics, Speech, Signal Processing (ICASSP) Conf.,* Vol.3, No.87, pp.147-149, 2002.

[7] A. M. M. Maamoun, M. Neggazi, and D. Berkani: "VLSI design of 2-D discrete wavelet transform for area efficient and high-speed image computing", *World Acad. Science, Eng. Technol.,* Vol.45, No.47, pp.538–543, 2008.

[8] I. Urriza, J. I. Artigas, J. I. Garcia, L. A. Barragan, and D. Navarro: "VLSI architecture for lossless compression of medical images using the discrete wavelet transform", *in Proc. Design, Automat. Test Eur.,* Vol.6, No.29, pp.196–201, 1998.

[9] M.Jiang, D. Crookes: "Area-efficient high-speed 3D DWT processor architecture", *Electron. Lett.* Vol.43, No.51, pp.502–503, 2007.

[10] M. Jiang, D. Crookes: "FPGA implementation of 3D discrete wavelet transform for real-time medical imaging", *in Proceedings of the 18th European Conf. on Circuit Theory and Design (ECCTD 2007), Seville, Spain,* Vol.3, No.67, pp.519–522 (2007).

AUTHOR BIOGRAPHIES

Kalavathi Devi.T, **She** received the B.E degree in and Electronics and Instrumentation Engineering from Government College of Technology, Coimbatore in 2002 and M.E degree in Applied Electronics from GCE, Salem in 2004. Currently, She is working as Assistant Professor Sr.G in the Department of Electronics and Instrumentation Engineering, Kongu Engineering College, Tamilnadu, India. She is a Life Member of ISTE, MIJSAT. He has received the best Teaching Staff award for the academic year 2011-12. Has published around 30 papers in conferences and journals. Her areas of interest include VLSI design and low power testing and Mixed Signal IC's.

Sakthivel.P, He received the B.E degree in Electrical and Electronics Engineering from Coimbatore Institute of Technology, Coimbatore in 1998 and M.E degree in Applied Electronics from Coimbatore Institute of Technology, Coimbatore in 2001. At present he is the Professor in the Department of Electrical and Electronics Engineering at Velalar College of Engineering and Technology, Tamilnadu, India. He is a Life Member of ISTE. He has received the best Teaching Staff award for the academic year 2003 & 2010. His areas of interest include Electrical Engineering, VLSI design and low power testing and soft computing Techniques

