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# A Crossbreed Cascaded Adder Architecture Using MATLAB Simulation

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## ABSTRACT

In early adder circuits the primary constraint was area, which led to development of simple scheme such as carry-skip, which improve the speed of addition while maintaining low gate-count. As technology scaling continued, several parallel prefix schemes like carries look ahead adder and Kogge stone adder are developed to yield fast adder design. The analysis of 16 bit Kogge stone adder is made designed using Weinberger and ling recurrence algorithm and the analysis based on some simulation parameters such as no of gates, power-delay product. The design of Kogge-stone adder has been carried out by using TANNER EDA tool. The efficiency of the adder design can be improved by prefix selection, algorithm, computational sum and logic depth. When Compared to Weinberger algorithm, the number of gates used is less in ling recurrence algorithm.

## 1. INTRODUCTION

Advances in CMOS technology have led to a improved significance in the design of basic functional units for digital systems. The portability requirement of hand-held computers and other portable devices places severe limitations on size and power consumption. Even though battery technology is improving continuously and processors and displays are quickly improving in terms of power consumption, battery life and battery weight is issues that will have a marked influence on how hand-held computers can be used. These devices often need real-time processing capabilities [1-11], and thus demand high throughput. The power consumption is becoming the limiting factor in the amount of functionality that can be placed in these devices. As technology scaling no longer achieves constant power density, the energy efficiency of functional units is of increasing importance to system designers.

Among the functional unit the adder is a basic block to apply the energy-efficient design methodologies. Because of the up gradation of technology and operating constraints have necessitated the refinement of adder implementation to obtain improvements in performance. To reduce the area occupied several simple schemes such as carry-skip was introduced to improve the speed of addition and to maintain low gate-count, then parallel prefix schemes were emerging to yield fast adder designs. In the earlier days because of transistor sizing there exists tradeoffs between speed and energy consumption so implementations must be compared by minimizing the circuit sizing and performance [12-44]. Nowadays energy efficient and addition algorithms were developed to yield better performance. However threshold voltages cannot be reduced ,static power consumption increases in the methods followed earlier, so improvements are to be made in the construction of adder, transistor sizing. Adders are not only used for addition, but are also used for implementing subtraction, multiplication, division, and address computation.

## 2. CMOS LOGIC DESIGNS

In CMOS (Complementary Metal-Oxide *Semiconductor*) technology, both N-type and P-type transistors are used to realize logic functions. Today, CMOS technology is the leading semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs). The main advantage of CMOS over bipolar technology is the much smaller power dissipation. Unlike bipolar circuits, a CMOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches [45-79]. This allows integrating many more CMOS gates on an IC than in bipolar technology, resulting in much better performance.

### *2.1. STATIC CMOS LOGIC*

The most commonly used logic style is Static Complementary CMOS logic. The static CMOS style really an extensive of the CMOS inverter to multiple inputs [80-115]. The most important advantage of the CMOS structure is robustness, good performance and low power consumption with no static power dissipation. Most of those properties are carried over to large fan-in logic gate implemented using in a similar circuit topology.

The output is connected to ground through an n-block and to Vdd through a dual p-block. Without changes of the inputs this gate consumes only the leakage currents of some transistors. When it is switching it draws an additional current which is required to charge and discharge the internal capacitances and the load. If *A* and *B* are both high, the output will be pulled low, whereas if one of *A* and *B* are low, the output will be pulled high. Most significantly, though, at all times, the output is pulled either low or high

### *2.2 DYNAMIC CMOS LOGIC*

Dynamic logic circuits are frequently faster than static counterparts, and require less surface area, but are more complicated to design, and have higher power dissipation. Dynamic logic is distinguished from so-called static logic in that it uses a clock signal in its implementation of combinational logic circuits. The basic construction of a dynamic logic gate, the pull down network (PDN) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases- “precharge and evaluation”- with the mode of operation determined by the clock signal.

The first phase, when Clock pulse is low, is called the setup phase or the precharge phase and the second phase, when Clock pulse is high, is Called the evaluation phase. In the setup phase, the output is driven high unconditionally (no matter the values of the inputs *A* and *B*). The capacitor, which represents the load capacitance of this gate, becomes charged. Because the transistor at the bottom is turned off, it is not possible for the output to be driven low during this phase. During the evaluation phase, Clock pulse is high. If *A* and *B* are also high, the output will be pulled low. Otherwise, the output stays high.

### *2.3. DOMINO CMOS LOGIC*

In this logic style system, the logic blocks are built with n-MOS pull-down tree that pre-charged and discharged through series clocking transistors. The output of the logic gate is driven by a build in inverter that is dynamically fed by the drain of the N-MOS tree is shown in Figure 3. When Clock pulse is low, dynamic node is precharged high and buffer inverter output is low. N-FETS in the next logic block will be off.

When Clock pulse goes high, dynamic node is conditionally discharged and the buffer output will conditionally go high. Since discharge can only happen once, buffer output can only make one low-to-high transition. When domino gates are cascaded, as each gate "evaluates", if its output rises, it will generate the evaluation of the next stage, and so on… like a line of dominos falling. Like dominos, once the internal node in a gate "falls", it stays "fallen" until it is "picked up" by the precharge phase of the next cycle.

## 3. KOGGE STONE ADDER

The Kogge-Stone adder [1] is an advanced parallel prefix form carry look-ahead adder. Kogge Stone adder is not limited in group size or number of levels for carry computation. It generates the carry signals in (log n) time [2], and is widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits. In KSA, carries are computed fast by computing them in parallel at the cost of increased area, but has a lower fan-out at each stage, which increases performance.

## 4. DESIGN METHODOLOGIES

The efficiency of Kogge Stone adder is further improved by the proper selection of following design methodologies.

- Algorithm
- Prefix Selection
- Logic Depth
- Conditional Sum

### *4.1. EXISTING ALGORITHM*

### *4.1.1. Weinberger Recurrence Algorithm*

The Weinberger recurrence algorithm was first developed by Weinberger. Weinberger established that addition speed could be improved by parallelizing the computation of carry [4]. Although widely credited with only the carry look ahead adder, Weinberger's recurrence was not limited in group size or number of levels of carry computation.

$$S_i = A_i \oplus B_i \oplus C_i \qquad (1)$$

$$C_{i+1} = A_i B_i + (A_i + B_i).C_i \qquad (2)$$

In Weinberger's recurrence algorithm, the carry propagation speed is improved through the use of generate and propagate. Propagate can either be implemented using an OR gate or an XOR gate. To differentiate them OR realization of propagate as transmit, *t*, and the XOR realization as, *p*. We define Weinberger's bit operations as

$$g_i = A_i B_i \qquad (3)$$

$$t_i = A_i + B_i \qquad (4)$$

Substituting into equation (2) obtains

$$C_{i+1} = g_i + t_i C_i \qquad (5)$$

Weinberger established that the recurrence algorithm applies to any prefix variation [5], through the use of group generate, *G*, and group transmit, *T in* Figure.1.

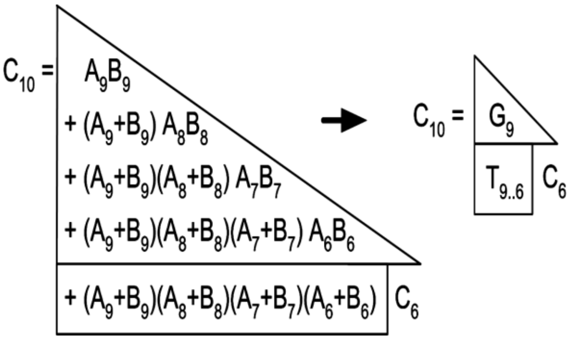

Figure 1: Weinberger's recurrence for addition

The computations of *G* and *T* are associative and idempotent, which allows for a wide range of recurrence tree possibilities for the carry computation. In Kogge-Stone, Han-Carlson [2] are most common recurrence tree variations for addition using Weinberger's recurrence as discussed in [3].The figure 1 shows that how to generate carry and sum for the addition using Weinberger recurrence algorithm.

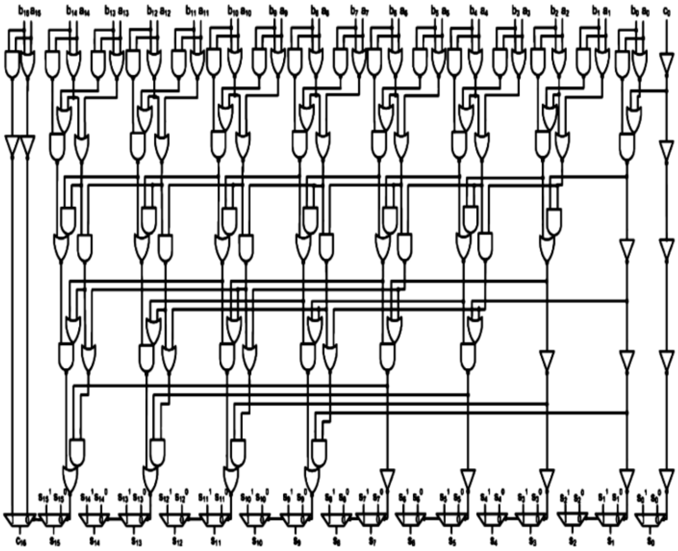

Figure 2: 16-bit kogge stone Weinberger adder

The Figure 2. Shows that the implementation diagrams for 16-bit kogge stone Weinberger recurrence adder structure. In this Weinberger structure number of gate used is more when compares to the proposed ling recurrence method.

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