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Low Pass Filter Using ECG Detection for OTA-C

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ABSTRACT

This paper Design Gm-c fourth order Butterworth filter for low pass filter for ECG detection. The filter strongly depends on basic building block such as transconductance cell, low power, highly linear. Pseudo differential Tran conductance cell working at 0.5 V in 180nm and n well CMOS technology. The gain of Tran conductance cell 57 db. Power consumption is 15 nw. The low pass filter with pass band gain 0 db. Cut off frequency 250Hz.Total power consumption is 157.5nW. The design implemented in TANNER TOOL 13.1 version to obtain the waveform.

Keywords: OTA, Pseudo-differential amplifier and Biomedical Application.

1. INTRODUCTION

Digital circuits to operate in low voltage, which serve low power dissipation. All physical signals are analog in nature. We need the analog interfacing module as front end circuit. Analog and digital circuit fabricate in same chip with increasing popularity of soc for miniature size. Analog circuit to operate in low voltage, which cause the performance degradation and leads technology development. Analog circuit to reduce channel length and Vth affect the performance. Operate low voltage will give optimum gain and signal swing of it low transistor stack, cost in common mode rejection. To overcome add extra circuit like common mode feed forward and common mode feedback. Local mode feedback circuit for improving input common mode rejection. To reduce the minimum supply voltage all transistor work in sub threshold region.

Improve the input dynamic range signal is connected to the bulk of PMOS and it operate in rail to rail operation well CMOS process forward biasing of PMOS bulk terminal. It is used to reduce the threshold voltage.to reduce the gain and bandwidth to bulk Trans conductance. Low power and frequency biomedical application transconductance cell is suitable. The Tran conductance cell is small. The operational transconductance amplifier (OTA) is an amplifier. The differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. To reduce the minimum supply voltage all transistor work in sub threshold region. MOSFET is using as an amplifier, input signal is given through gate terminal of the MOSFET. The bulk is tied to the bias voltage. This technique is called gate-driven in which output current is a function of input gate-to-source voltage.

The OTA is similar to Operational amplifier. It has a high impedance differential input stage and that it may be used with negative feedback. Design the cut off frequency 250 Hz that RC time constant. To implement of large rand c on soc is may not be cost effective solution .Implementation large R, Gm-c filter with low transconductance in 180nm technology. Design butterworth low pass filter the filter value is 1PF to 10 PF. The c-value need for design very low Gm getting required cut-off frequency. Gate driven, bulk driven input will reduce Gm by 4 to 5 times. Further to reduce Gm to use the conventional method like current division, current division, current cancellation,

source degeneration. This are fail PDA operate low supply voltage .Reduce Gm to use capacitor multiplier technic is presented. To increase the time constant. Large supply voltage dynamic range improved expanse of increase the power consumption. The portable device the ultra low power operation is a main requirement leads low supply voltage.

2. OPERATIONAL TRANSCONDUCTANCE CELL

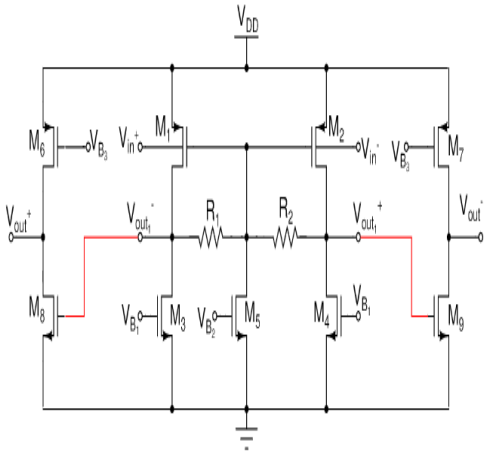
This section presents design of ultra low power Gm cell used for large time constant Gm-C filter. For working in low supply voltage of 0.5 V, a pseudo-differential architecture is designed. For getting a low Gm of around 20 nS, the Gm cell circuit is designed. Ultra low power Gm cell designed used for large time constant Gm-c filter .Design pseudo differential architecture Gm value is 20ns. In the first stage of OTA input is connected to bulk of the PMOS transistors M1 and M2.The NMOS transistors M3 and M4 are act as current source load for first stage of OTA.

It getting a good dynamic range at input, input common mode voltage of 250 mV. It circuit take half of the supply voltage. For proper operation of OTA cell while cascading to next stage, the output common mode voltage should be same as the input common mode voltage. By passing the current through the transistor M5, the drop across the resistors R1 and R2 set the output common mode voltage of 250 mV. In the ideal OTA, the output current is a linear function of the differential input voltage, calculated as follows:

$$I_{\text{out}} = (V_{\text{in+}} - V_{\text{in-}}) \cdot g_{\text{m}}$$

Where V_{in+} is the voltage at the non-inverting input, V_{in-} is the voltage at the inverting input and g_m is the transconductance of the amplifier.

3. BLOCK DIAGRAM FOR BULK DRIVEN OTA



The common mode feedback provided by the resistors R1 and R2 and the transistor M5 improves the input common mode rejection ratio .The resistors R1 and R2 are implemented using PMOS transistors in linear region.

The bias circuits are not presented in the paper. The equation for differential and common mode gain for first stage is

$$A_{diff1} = \frac{g_{mb1}}{g_{ds1} + g_{ds3} + \frac{1}{R_1}} \qquad (1)$$

$$A_{cm1} = \frac{g_{mb1}}{g_{ds1} + g_{ds3} + g_{m1}} \qquad (2)$$

Since input is connected to bulk of terminal of PMOS transistor in first stage, the gain of that stage is very less. A common source amplifier with current source load is connected at the second stage to enhance gain. The second stage will give an additional gain as given in (3). The negative (positive) output of first stage is connected to the NMOS M8 (M9) and the PMOS transistor M6 (M7) act as current source load. For using same bias circuitry for all bias voltages VB1 , VB2 and VB3 , fixed all bias voltage to a single value 250 mV.

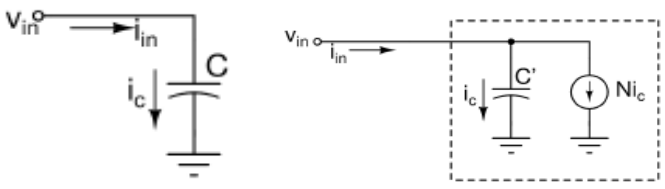
$$A_{diff2} = \frac{g_{m8}}{g_{ds6} + g_{ds8}} \qquad (3)$$

The two stage OTA gives a pass band gain of 57 dB and unity gain band width of 3.18 kHz with a load capacitance of 1.

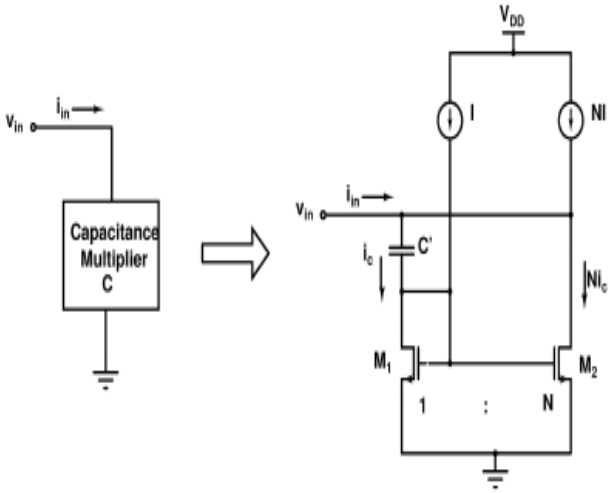
4. CAPACITANCE MULTIPLIE

A capacitance multiplier is designed to make a capacitor function like a capacitor that is much larger. This can be achieved in at least two ways. An active circuit using a device such as a transistor or operational amplifier. A passive circuit, using auto transformers. The capacitor multiplier working is based on the principle scaling impedance. Or admittance from required port. Capacitor increase the reactance across the capacitor for particular voltage and more current. The more current produce the same voltage lead to decrease the impedance three by large capacitor is used. The capacitor is used to reduce the area but expense of more power.

a) Single capacitor **b) Multi capacitor**



c) Circuit implementation of capacitor multiplier



5. LOW PASS FILTER ARCHITECTURE

Cascading two biquad filter implementation a 4th order Butterworth filter .provide the a roll off factor of 80 dB per decade.to avoider voltage saturation output side to increase the dynamic range. The cascade filter in the decreasing order of damping ratio. The quality factor and Damping ratio are inversely proportional. The butterworth filter required quality factor of first and second stage is 0.54 and 1.31.

A low-pass filter (LPF) is a filter that passes signals very low frequency. This frequency lower than a certain cutoff frequency. The attenuates signals with frequencies higher than the cutoff frequency. A low-pass filter is the complement of a high-pass filter. The equation given below cut off frequency and quality factor.

$$f_o = \frac{1}{2\pi}\sqrt{\frac{G_{m3}G_{m4}}{C_1C_2}} \qquad (5)$$

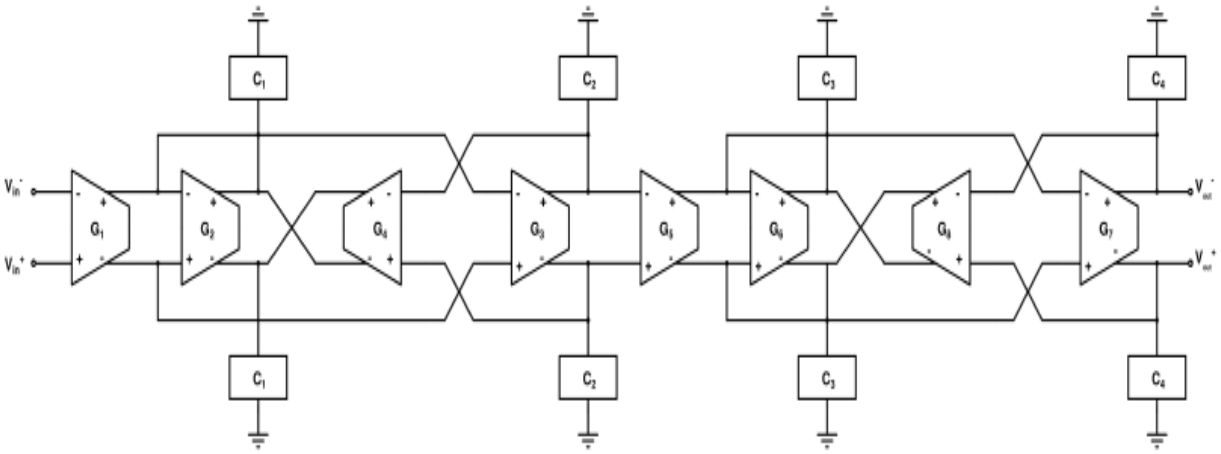
$$Q = \sqrt{\frac{G_{m3}G_{m4}}{G_{m2}^2}}\sqrt{\frac{C_1}{C_2}} \qquad (6)$$

All Gm cell used in circuit are identical of transconductance 20 nS. So the above equations reduced to (7) and (8).

$$f_o = \frac{1}{2\pi}\frac{G_m}{\sqrt{C_1C_2}} \qquad (7)$$

$$Q = \sqrt{\frac{C_1}{C_2}} \qquad (8)$$

For getting a cut off frequency of 250 Hz and desired Q values for maximally flat response, design the capacitance values by fixing Gm of 20 ns. For implementing large value capacitance, by using the capacitance in the range of 1 pF to 10 pF, need to use capacitance multiplier.



Fully Differential Fourth Order Butterworth LPF

6. RESULT

0.5 V two stage pseudo-differential OTA is used to simulate a fourth order fully differential Butterworth filter in TANNER EDA TOOL. The OTA cell is having a transconductance value of 20 nS by consuming power 15 nW. Operating supply voltage is 0.5 V. A pass band gain of OTA is 57 dB .The unity-gain frequencies of 3.183 kHz for 1 pF load capacitance. The power dissipated by LPF with capacitance multiplier is 157.5 nW. For implementing a total capacitance of 56.85 pF, capacitance multiplier utilizes the total mim capacitance of 19.83 pF at the expense of 37.5 nW additional power. Therefore area used to implement mim capacitance is reduced by a factor of about 3 compared to the circuit without capacitance multiplier.

SUMMARY AND COMPARISONS OF LOW PASS FILTER FROM THE LITERATURE SURVEY

Parameter	Ref [5]	Ref [6]	Ref[7]	Ref [8]	This work
Supply Voltage (V)	3	1.25	3	1	0.5
Technology (nm)	180	800	180	180	180
Bandwidth (Hz)	2.4	2000	37	250	250
Order	6	6	5	5	4
Power	10uW	2.5uW	453uW	2.5uW	157.5uW
THD (dB)	-60	-40	-61	-48	-50
DR (dB)	60	70	57	50	54
FoM (pJ)	1920	0.0425	15.2	0.1449	0.05383
Filter structure	Gm-C	Gm-C	Gm-C	Gm-C	Gm-C

FIG 1: LINEARITY OF THE OTA CELL

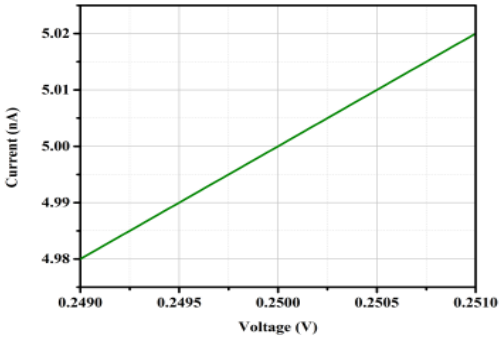
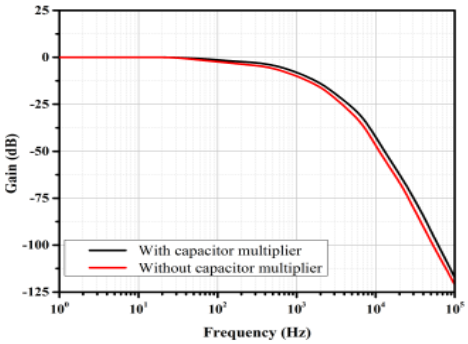
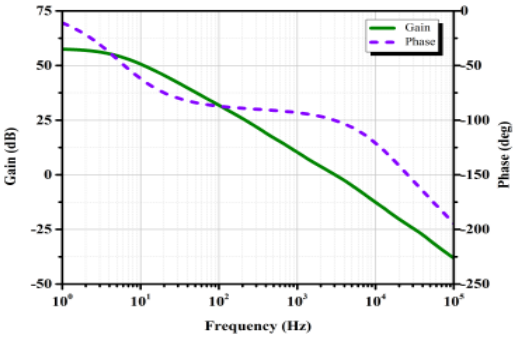
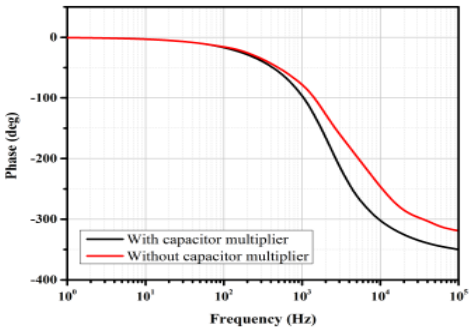


FIG 2. MAGNITUDE RESPONSE OF LPF







7. CONCLUSION

0.5V two stage pseudo differential OTA is used to stimulate fourth order fully differential butterworth filter. OTA transconductance value is 20ns consuming 15nW power with supply voltage of 0.5 V. The Pass band Gain is 57Dband the operating frequency 3.183KHz.The load capacitance value 1 PF .The Power dissipated by low pass filter with.

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