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Implementation of Sleep Transistor Based SRAM Using Resonant Supply Boosting For Low Power Application

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ABSTRACT

This paper presents a novel resonating inductor based supply boosting scheme for low-voltage static random-access memories and logic in deep 14-nm silicon on insulator (SOI) FinFET technologies. The technique combines capacitive (C) and inductive (L) boosting for the first time. Simulation and measured hardware results from a 14-nm test chip show that this new technique is able to improve Vmin (down to 0.3 V), functional yield, and access time, when compared with designs with or without capacitive-boosted supplies. Simulations also reveal the optimal combinations of "L" and "C" needed for each Vdd to achieve minimal boost voltage, where the static random-access memory can be rendered fully functional in the absence of any assist circuitry. Furthermore, the resonant supply provides power savings compared with a boosted supply alone.

Keywords: Boosted supply, FinFet, Inductors, Low-power electronics, Low Vmin, 8T and Static random-access memory (SRAM).

1. INTRODUCTION

Embedded static random-access memories (SRAMs) are still the workhorse of the VLSI industry. Being the smallest in size and the densest structures on a chip, SRAM represents a critical portion of most microprocessor and system on chip designs. Decades of effort have been spent lowering power and maintaining functionality in these designs as the technology scales. There are various techniques listed in the literature to lower the power of SRAMs. Some of the notable ones are static and dynamic dual power supply, usage of multi-Vt devices for the cell, shorter bit lines, usage of write assist techniques, the addition of transistors in an SRAM cell, and the usage of technology, e.g., silicon on insulator (SOI) versus bulk and non-planar versus planar. The power supply remains one of the key knobs for reducing power consumption; however, lowering the power supply requires a balancing act for maintaining Vmin in order to achieve functionality as well as the performance of SRAM cells and latches. Functionality here can be best described in terms of cell write ability, read stability, and data retention, which strongly depend on process, voltage, and temperature variations. Furthermore, for high performance processors, it is important to maintain wide range of operation from low to high Vdd to achieve the optimal power and performance operating point for the given situation.

The operation of SRAM arrays at near threshold voltages still poses a challenge due to variability and functional yield difficulties when lowering supply voltages. Researchers have proposed techniques to improve stability for conventional 6T/8T cells, which include dual static as well as dynamic power supply boosting techniques using charge pumps and assist techniques targeting specifically arrays.

However, many of these techniques result in area, power, and/or supply voltage penalties. Recent trends show that static and separate power supplies are commonly used for arrays. The approach of using a static dual supply for the SRAM cell, the wordline, and/or the logic comes at the cost of an extra power supply that adds complexity to the design as well as power. As an alternative to static dual supply, a charge pump methodology was proposed to boost

only the word line however, extending this approach to the entire array would increase area and power. Likewise, the word line may be dynamically boosted supply with a 50% duty cycle To alleviate some of the power consumption overhead of a 50% duty cycle boost, “a step-down” dynamic word line boost is applied to only word line drivers with a much reduced duty cycle ,While this step-down approach reduces power, the lower voltages may lead to SRAM arrays functionality issues, which get worse as the desired beta and gamma ratios of SRAM cells cannot be achieved in scaled technologies and especially in FinFET technologies.

Integrated read- and write-assist techniques utilizing word line under drive and cell voltage collapse are often used for 6T SRAM macros. However, with these techniques, the demonstrated voltage retention time is reduced to 1.6–4.2 ns depending on the threshold voltage of the pFET. Write-assist techniques utilizing reduced bit line voltages or negative bit lines are often used for achieving write ability, although they do not help to improve performance especially when Vmin is lowered. Furthermore, negative boost swings for an individual or a group of bit lines need assist circuits, which come as a power cost. Usage of dynamic voltage collapse-assist techniques also helps write ability; however, cell operation becomes difficult at extremely low voltages

Many of the above-mentioned techniques employ planar technologies. The recent advent of FinFET technology and its application to processors have helped to lower operating voltages slightly used. Although FinFET technology is attractive for low-power applications, many new circuit innovations are still needed to lower Vmin for memory as well as logic. Also, many of the prior techniques listed previously are localized to either word lines or arrays, and do not fully resolve the simultaneous requirements for functionality, performance, yield, and Vmin of SRAMs. Although much of the work reported in advanced technologies is on bulk technology, SOI offers many attractive qualities from a technology perspective, including vertical etched fin profiles and soft-error rate advantages over bulk. In this paper, we exploit 14-nm SOI FinFET technology as well as novel circuits and interconnect structures to lower the operating voltage while maintaining performance at higher voltage. We introduce two novel concepts for on-demand power supply boosting:

1) capacitive coupling with interconnects and
2) capacitively coupled inductive boosting.

The techniques we propose can be applied to memory as well as logic, and mitigates many of the overheads of the prior art. Recently, we have proposed a voltage-supply boosting technique that leverages the inherent capacitance in a FinFET device to boost the supply voltage and improve SRAM operation. In this paper, we develop another concept by adding an inductor between a new standard cell-based boosting circuit and the virtual supply voltage grid to the macro. Conventionally, parasitic inductance has been considered problematic for digital circuits, leading to mitigation techniques. More recently, however, techniques such as resonant clocking have explicitly added inductors to induce resonant behaviors for power savings. Our new inductor-based supply boosting technique not only leads to power reduction, but also improves our prior supply boosting technique in terms of Vmin, access time, and yield. Table I provides a comparison of our proposed inductor-based supply boosting technique and prior

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works. While it is difficult to directly compare designs that may differ in target objectives and technologies, it is clear that our proposed technique advances the art significantly in terms of Vmin and novel, simplified solutions.

2. LITERATURE SURVEY

Eric Karl et al. proposed a 0.6–1.1 V, 84 Mb pipelined SRAM array design implemented in 14 nm FinFET CMOS technology is presented. Two array architectures featuring a high-density 0.0500 μm2 6T SRAM bit cell and a 0.0588 μm2 6T SRAM bit cell targeting low voltage operation are detailed. The high-density array design reaches 2.7 GHz at 1.1 V with 14.5 Mb/mm2 bit density, while the low voltage optimized array can operate at 0.6 V, 1.5 GHz under typical process conditions. A capacitive charge-share transient voltage collapse write-assist circuit (CS-TVC) enables a 24% reduction in write energy compared to previous techniques by eliminating bias currents during operation. Technology and assist co-optimization enable 50 mV reduction in V and a 1.81× increase in density over a 22 nm design.

Jaydeep Kulkarni et al. discussed about the High-performance microprocessors and SoCs include multiple embedded memory arrays used as register files and low-level caches that typically share the same supply voltage as the core. The desire for wide voltage range operation to optimize power and performance dictates the need for SRAM arrays that can achieve both high performance and low minimum voltage of operation (VMIN). The 8T bit cell is commonly used in these applications because its decoupled read and write ports offer fast read (RD) and write (WR) operations with generally lower VMIN than the 6T bit cell. However, process variations result in mismatches between the pull-up and access devices limiting write VMIN, and/or between read port and keeper transistors limiting read VMIN. Traditional device up-sizing provides diminishing returns at a large area and power cost.

Harold Pilo et al. proposed a 64 Mb SRAM macro has been fabricated in a 32 nm high-k metal-gate SOI technology. The SRAM features a 0.154 m bit-cell, the smallest to date for a 32 nm SOI product. A 0.7 V operation is enabled by three assist features. Stability is improved by a bit-line regulation scheme which reduces charge injection into the bit-cell. Enhancements to the write path include an increase of 40% of bit-line boost voltage. Finally, a bit-cell-tracking delay circuit improves both performance and yield across the process space.

Koichi Takeda et al. proposed a multi-step word-line control technology (MWC), combined with a new hierarchical cell SRAM architecture (HCA), has been developed to overcome rapid increase in random variability with no area penalty. A 40-nm-node 0.248- m-cell SRAM using a single power supply has been successfully fabricated, pushing up bit density to 2.98 Mb/mm. MWC improved VDD min at-6 by 0.34 V and 0.22 V for read and write operations, respectively, enabling stable 1.0 V operations. Four nanosecond SRAM access time is achieved by adopting HCA, which cancels out a 1.4 ns increase of access delay caused by MWC.

Rouwaida Kanj et al. proposed a novel methodology for statistical SRAM design and analysis. It relies on an efficient form of importance sampling, mixture importance sampling. The method is comprehensive, computationally efficient and the results are in excellent agreement with those obtained via standard Monte Carlo techniques. All this comes at significant gains in speed and accuracy, with speedup of more than 100X compared to regular Monte Carlo. To the best of our knowledge, this is the first time such a methodology is applied to the analysis of SRAM designs.

3. BACKGROUND METHODALOGY

In this section, we describe dynamic supply boosting techniques to enable extreme low-voltage operations showcasing a 14-nm 8T SOI FinFET SRAM, including a peripheral logic. We describe two novel concepts for on-demand power supply boosting. First, we introduce a base technique employing capacitive coupling of a FinFET device and interconnects to boost Vdd. Second, we build upon the base technique by adding an inductor to the boosting structure, which is presented for the first time in this paper.

BOOSTING VIA CIRCUIT LEVEL CAPACITIVE COUPLING

The base technique exploits the unique capacitive coupling effect in a FinFET device to dynamically boost the virtual macro supply voltage during active mode, thus improving the access performance and Vmin in the presence of variability. We also utilize interconnects to increase the capacitive coupling and thereby boost the power supply for the full macro. A negative bitline write-assist technique is also incorporated to further improve write-ability yield technique is also incorporated to further improve write-ability yield. The proposed scheme requires only a single supply and exploits the capacitive coupling from the gate and channels of a FinFET to its source as shown in Fig. 1. The basic circuit consists of two opposite polarity FETs in parallel with drains connected to Vdd. The boost transistor consists of an n-type FinFET with its gate controlled by the "BOOST" signal. Their common source forms a virtual Vdd (Vddv). In standby, BOOST is "Low", thus the virtual array supply voltage is at Vdd.

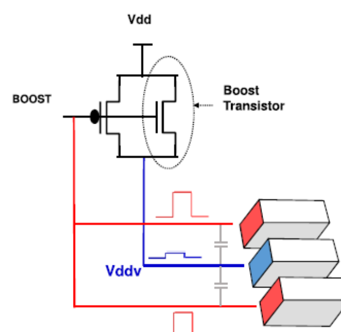

Fig.1. Transistor boosting and interconnect boosting

In this technique is also incorporated to further improve write-ability yield. The proposed scheme requires only a single supply and exploits the capacitive coupling from the gate and channels of a FinFET to its source as shown in Fig. 1. The basic circuit consists of two opposite polarity FETs in parallel with drains connected to Vdd. The boost

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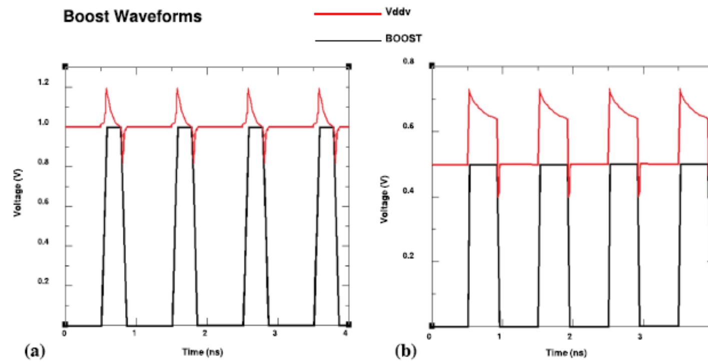


Fig. 2. Boost waveforms at (a) high voltage supply and (b) low voltage supply

Fig. 2 shows physics-based technology computer-aided design simulations to demonstrate the boost at short and long pulses with high and low voltages. One key aspect that is evident from Fig. 2 is that the relative Vddv increase is higher at lower Vdd, making this technique attractive for improving Vmin and performance at lower Vdd.

4. RESULT AND DISCUSSION

Fig. 3(a) shows the new capacitively coupled inductor based boosting scheme. In this case, the device-based capacitor circuit provides the initial boost to "Vddv," which then gets further boosted by an appropriately sized inductor. The detailed analysis will be shown in Section III. The explicit inductor and inherent macro capacitance creates an LC tank that can be used to resonate and overshoot the supply, depending on the "L" and "C" values.

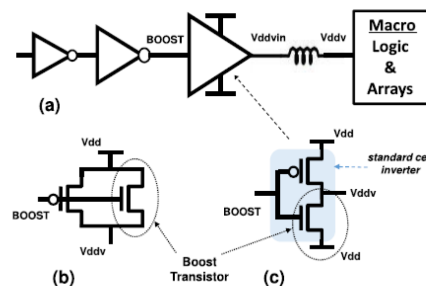


Fig. 3. (a) Inductive-based boosting concept. (b) Custom booster [4]. (c) Inverter-based booster.

STANDARD CELL-BASED BOOSTING STRUCTURE

The booster circuit is a novel design employing a standard cell inverter, opening the door to a more general application of supply boosting. In our previous work the boost circuit was designed by modifying the existing pFET header structure in the SRAM array macro to include an additional nFET boost transistor [Figs. 1 and 3(b)], requiring a full custom layout change, but leading to a low area overhead of approximately 4%.

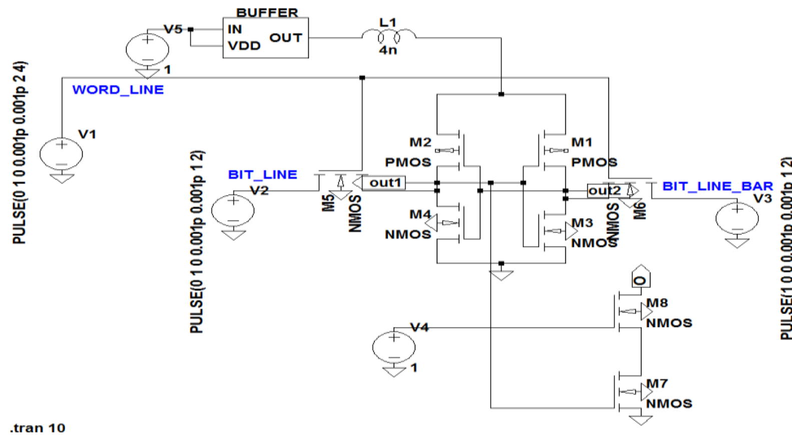


Fig 4. Schematic diagram of voltage level boosted SRAM cell

The test chip in this paper, however, employs an SRAM macro that does not include a pFET header, prompting a new approach using a standard cell inverter, where the Nfet source connects to Vdd [Fig. 3(c)], leading to a structure identical to the custom booster in Fig. 1. The inverter-based boost cell and prior gain inverters are then wrapped around the SRAM array macro. This new booster cell approach, consisting only of standard cells, provides a solution for boosting any array or logic macro at a reduced design effort cost and even lays a direction for full automation via synthesis tools.

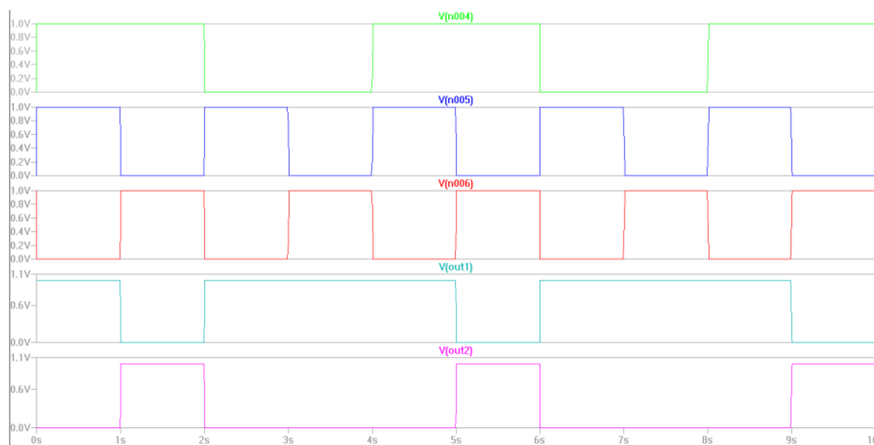
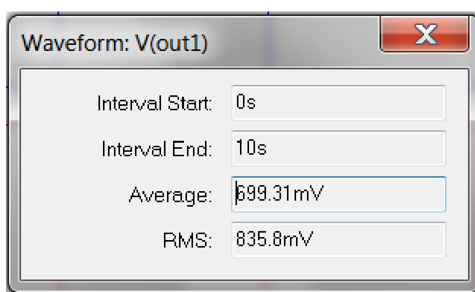


Fig 5. Output waveform of voltage level boosted SRAM cell



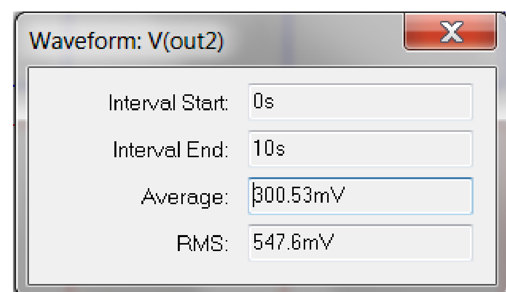


Fig 6. Average and RMS voltage of Output1 1and 2

Fig. 5 shows simulated boosted Vddv waveforms for two voltage and frequency pairs, with and without the new inductor technique. These simulations both use a 4-nH inductor and illustrate the range of Vddv waveforms that can be generated. For this example, the value of the inductor is so chosen for functionality at ultralow Vmin. Similar to other techniques that employ inductors for digital design, e.g., resonant clocking, it is important to size the inductor for the target cycle time range and/or provide multiple inductors for dynamic selection. In resonant clocking, boosting is not the primary motivation, while in this application boosting and recycling charge is a key for functionality and lower power.

There are also numerous refinements to the proposed technique, such as, adding a diode to limit undershoot below Vdd, although these variants are beyond the scope of this paper. Fig. 6 shows how inductor-based boosting with an appropriately sized inductor provides correct operation at low voltages without write-assist circuitry [Fig. 6]. Without boosting, even the write-assisted case leads to incorrect functionality [Fig. 6], while the case of boosting with a 2-nH inductor requires write-assist for correct functionality [Fig. 6].

The 4-nH inductor provides an initial boosted pulse with higher and wider amplitude than the 2-nH inductor, providing functionality even without write assist. The voltage overshoot provided by a properly sized inductor improves the device strength of the word line and cell, allowing the writing. Fig. 8 shows an access time comparison between various inductor sizes, where the boost with inductor gives lower access time in general. Out of these inductors, 4 nH shows slightly higher delay for the same boost circuit, but it is capable of lowering Vmin to 0.3 V compared with other techniques without any additional circuitry. In terms of power consumption, as the inductor size increases, the average power decreases compared with boost alone due to oscillating “LC” characteristics.

For 8T cell functionality, write ability is a key parameter to be evaluated. Write-ability failure is defined if the node “0” to be written by “1” does not reach 90% of Vdd during active word line pulse width. With respect to yield, the write-ability yield using a super fast high-sigma technique. Using key mismatches as the input and the mixture important sampling technique described in [21], the high-sigma regime is explored in Fig. 10. This plot highlights that at low Vdd the 4-nH inductor has over three units higher yield than without boost and 1 unit over boost alone. Usage of the optimal “L” and “booster capacitance” allows the boost voltage to be sufficiently higher than the one required for the write-ability criterion.

5. CONCLUSION

In summary, the new inductor-based boosting technique shows promising results for improving Vmin, access time, and power consumption. This novel resonant supply boosting concept was explored through theoretical modeling, simulation, and measured hardware. The 14-nm FinFET SOI test chip measurement results verify simulations, suggesting improvements over the capacitive boosting technique alone. Although this paper provides only an initial

investigation into resonant supply boosting, there are numerous avenues to further optimize the proposed technique, which may be beneficial for future low power processors, accelerators, and IoT applications.

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