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Design of Sigma-Delta Analog-To-Digital Converter by Using Low Power 0.25 µM CMOS Comparator

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ABSTRACT

Power consumption is the important parameter in VLSI circuits. To reduce the power consumption of the circuit many methods are proposed in the past. The channel length modification is the important measure. A CMOS comparator using dynamic latch, suitable for high-speed Analog-to-Digital Converter (ADC) with high speed and low power dissipation is presented. This design is planned to be proposed in Sigma-delta ADC. This circuit combines the good features of the resistive dividing comparator and the differential current sensing comparator. The design has been carried out in Tanner EDA tools, the schematic simulation is done using Schematic Editor (S-Edit) and layout simulation of the design is verified using Layout Editor (L-Edit) using 0.25µm CMOS technology. The Simulation results are verified with supply voltages of 1.6V, 1.8V and 2.0V respectively. It is found that the power is least dissipated in 1.6V which is 0.7899 mW, but it has the longest propagation delay of 0.715 ns. In contrast, the 2.0V supply produced 1.471 mW and a shorter delay of 0.550 ns.

Keywords: Power consumption, VLSI circuits and Schematic Editor.

1. INTRODUCTION

Modern technology in research and development of the Complementary Metal Oxide Semiconductor (CMOS) has led to great reductions in the size and power consumption of modern electronic circuitry. There are many proposed topologies on how the technology should be distributed which aim to minimize the power consumption and maximize the data transfer [1]. Now a days mostly we are using Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) circuits because of the need to translate analog signal to digital signal and vice versa. A comparator plays a basic role in most electronic applications. Due to the large number of comparisons in some ADC structures, such as flash ADCs, the speed and the power consumption of the comparator have important influences on the performance of ADC [2]. High speed ADC is the key component in the area of analog and/or digital interface with the increasing demands for a high speed ADC. At the same time, the speed of the comparator is the main factor to the speed of the ADC [3]. A high speed ADC is very critical in some digital system and with the requirement to prolong the battery life of the system; a comparator with low power consumption is needed.

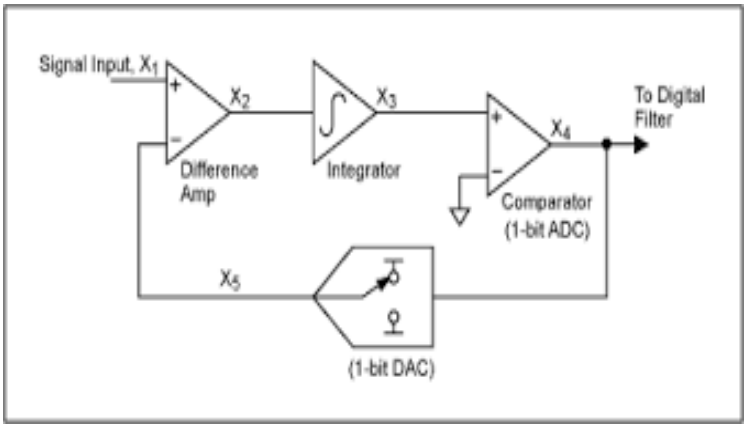

Fig 1. Sigma delta ADC

There are many types of ADC available nowadays, example like Flash ADC, Sigma Delta ADC, dual slope converter an successive approximation converter. One of the more advanced ADC technology is the Sigma Delta ADC or ΔΣ. Sigma Delta is one of the analog to digital converters which are ideally for converting signals over a wide range of frequencies from direct current to several megahertz with a very high resolution results.

The Analog to Digital Converter (ADC) converts the mean of an analog voltage into the mean of an analog pulse frequency and counts the pulses in a known interval so that the pulse count separated by the interval gives an perfect digital representation of the mean analog voltage during the interval. This intermission can be chosen to give any desired resolution or accuracy. The method is cheaply produced by modern methods; and it is widely used.

In sigma delta modulation, the analog signal is quantized by a one-bit comparator. Output of the comparator is changed back to an analog signal with a 1-bit DAC, and subtracted from the input after passing through an integrator. Thus, a good comparator design is the focused of this paper.

2. *MATHEMATICAL ANALYSIS*

A. Propagation Delay

Propagation delay is the time required by the input to produce the corresponding change in the output signal [4, 5]. The propagation delay in the comparator generally varies as a function of the input. The shorter the propagation delay, the higher the speed of the circuit and vice-versa. A larger input voltage will result in a smaller delay time. the propagation delay, or gate delay, is the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. The propagation delay of a comparator can be express as in equation (1):

$$\text{Propagation delay} = (\text{tplh} + \text{tphl})/2 \quad (1)$$

Where
tphl = delay time when output change from high to low
tplh = delay time when output change from low to high

B. Speed

Speed is the inverse of the propagation time delay. The speed of a comparator can be calculated using equation (2):

$$\text{Speed} = 1/(\text{propagation time delay}) \quad (2)$$

C. Power Dissipation

Power dissipation is the rate at which energy is dissipated from electrical circuits. It is measured in watts. Dynamic comparator power dissipation is given approximately by equation (3):

$$\text{Power} = f \times C \times V_{DD}^2 \qquad (3)$$

Where

1 = output frequency

V_{DD} = the supply voltage

C = output capacitance

For high frequency circuit operation, the trade-off must be made between speed and power dissipation. Speed will be mainly affected by the slew rate requirements and load impedance. The lower the load resistance, the more current will be needed to achieve the desired speed of operation. The gain of the comparator will influence the speed and the power dissipation. The gain can be increased by increasing the power supply voltage.

3. PROPOSED DESIGN

In the future circuit, the proposal is to combine the charge sharing comparator and output buffer circuit. The comparator combines the features of both the resistive dividing network and differential current sensing comparator. Therefore, the comparator consists of two stages. Figure 1 shows the charge sharing topology for the dynamic latch comparator circuit. In Figure 1, resistive comparing circuit for regenerative mode is used in series with NMOS transistor NMOS_9 in order to get a low power consumption. Besides that, PMOS transistor for pre charging circuit is absent during reset mode and NMOS transistor NMOS_1 for output pass transistor is nearly to Vdd/2 for the equalization of both voltage. The latch now is disconnected from Vdd and ground with the aid from transistor PMOS_1 and NMOS_9.

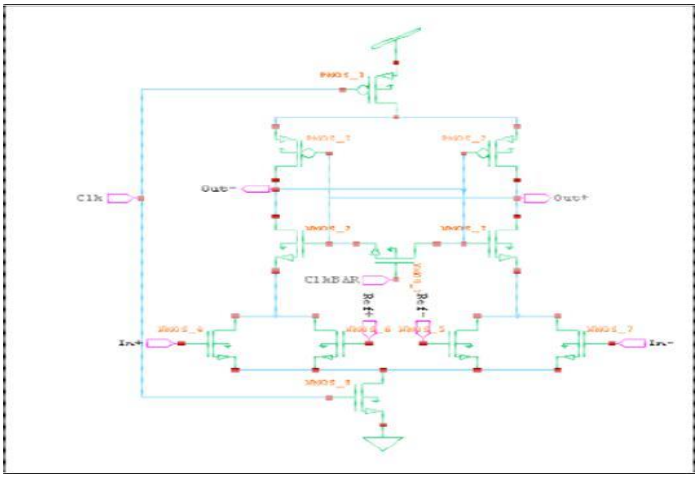

Fig. 2. Charge sharing topology for dynamic latch comparator

Figure 2 shows the output buffer circuit. This circuit is also known as post amplifier. Basically, the circuit receives the information from the latch and produces a digital output signal. The output buffer stage consists of a self-biased differential amplifier followed by an inverter which gives the digital output. The digital output converts the output

of the latch stage to a full scale digital level output (logic 1 or logic 0). The output buffer stage should be able to accept a differential input signal (Out + and Out-from the charge sharing circuit and will not have slew-rate limitations.

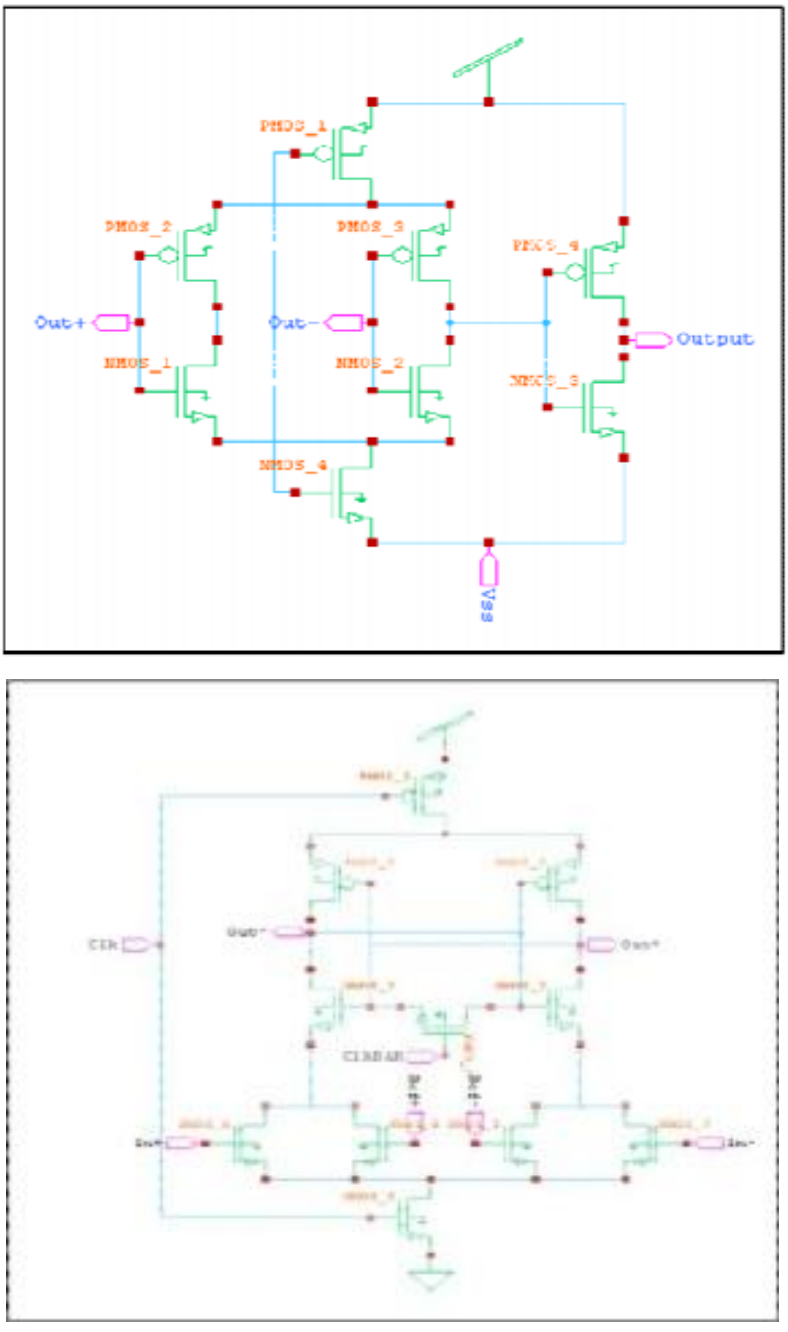

Fig. 3: Output buffer circuit

4. SIMULATION AND RESULT

The schematic of the dynamic latch comparator is shown in Figure 3 which consists of both stages which are the dynamic charge sharing comparator along with the output buffer stage. Now, the two ended output of dynamic charge sharing comparator (Out+ and Out-) in Figure 1 become the input to the buffer circuit in Figure 2. Thus,

making the two ended output of dynamic charge sharing comparator is being converted into single ended output which is labeled as output.

Transistor sizing is important in ensuring the correct output of the comparator [6]. Table 1 shows all the sizing of the transistors used in this design. It is based on CMOS technology of 0.25 µm. The right sizing is critical and will also affect the speed of the circuit.

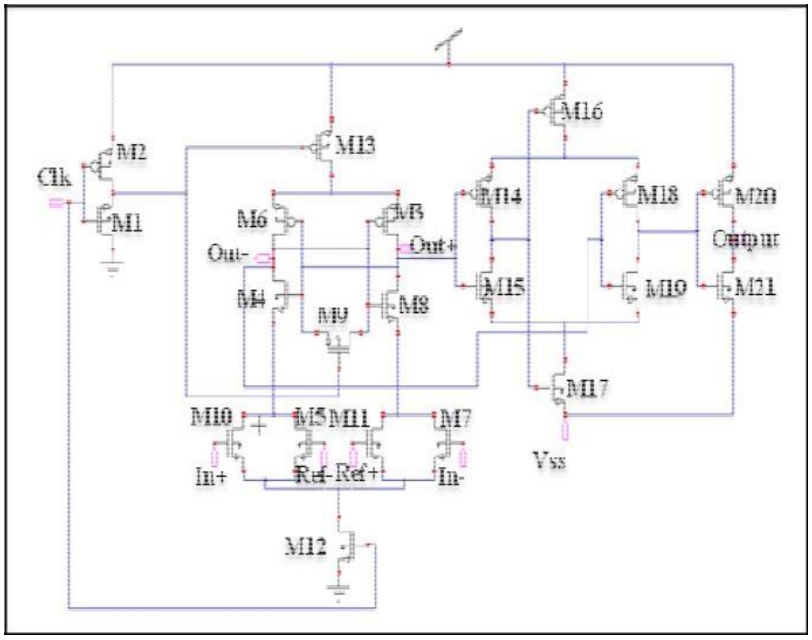

Fig. 3: Proposed dynamic comparator circuit

Table 1. Transistor dimension (µm) of the dynamic comparator circuit in Figure 3.

Transistor	**Technology**
	0.25 µm
M1, M4, M5, M7, M10, M11	5
M2, M3	10
M6, M13, M14, M16, M18, M20	8
M8, M9, M12, M15, M17, M19, M21	4

The circuit in Figure 3 is tested with a supply voltage of 2.0V, 1.8V and 1.6V respectively. The reference Voltage is +1 V and -1 V.

5. TRANSIENT ANALYSIS

For the transient response, the input voltage sources (In+ and In-) are a pulse voltage sources and the reference voltage sources are a DC voltage sources. The input signal is compared with the reference voltage during evaluation mode (Clk = 1). When the input signal voltage (In+ or In-) is greater than the reference voltage (Ref+ or Ref-), the output (Out+ or Out-) is high and vice versa. Besides that, it is also found the output (Out+ and Out-) nodes are 180˚ (degree) out of phase to each other. The comparator converted the input voltage (V_{IN}) into logic "1" or "0" by comparing the VIN with a reference voltage (V_{REF}). If V_{IN} is greater than V_{REF} the output is "1'', otherwise it is "0".

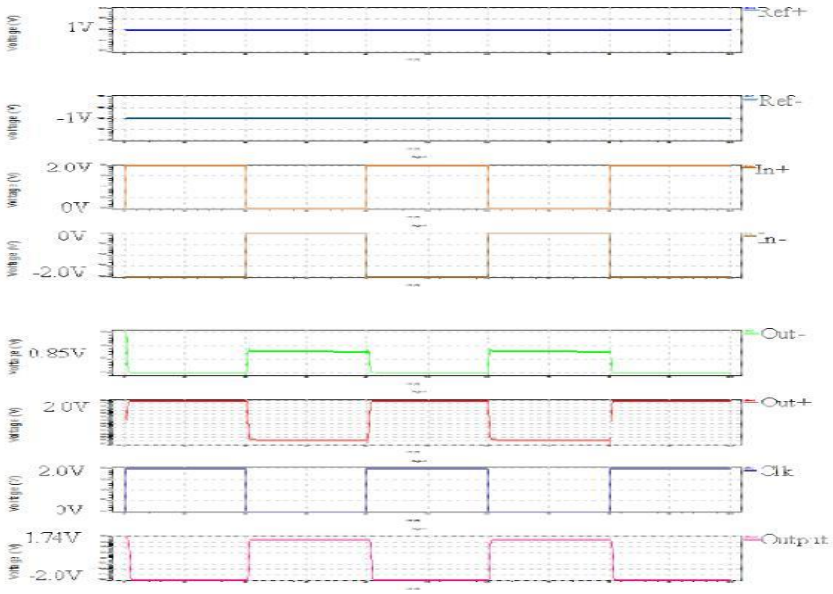

Fig. 4. Transient response of dynamic comparator circuit using power supply of 2.0V.

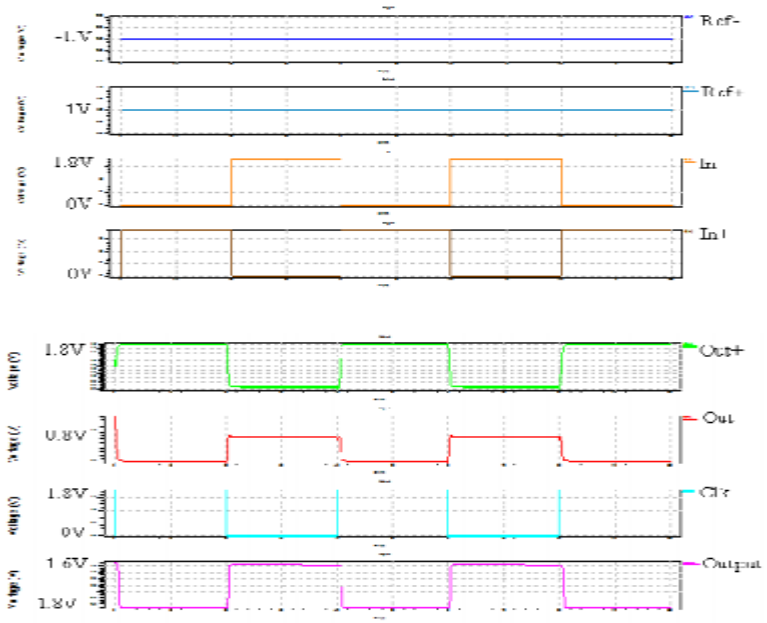

Fig. 5. Transient response of dynamic comparator circuit using power supply of 1.8V.

Figure 4, 5 and 6 show the transient response of the designed comparator using 0.25 µm technology, for a 2.0V power supply, 1.8V and 1.6V respectively. The results show that the comparator is working perfectly even though different power supply is applied. As compared to the result in [7], the proposed circuit can work better because it can be operated with a power supply as low as 1.6V with a correct output and using a smaller CMOS technology.

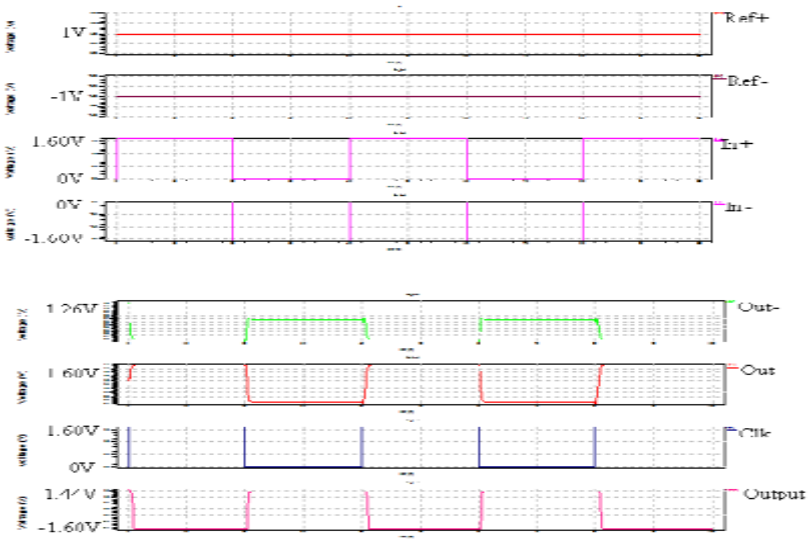

Fig. 6. Transient response of dynamic comparator circuit using power supply of 1.6V

6. DELAY ANALYSIS

Figure 7, 8 and 9 prove the delay in the output waveforms with different power supply. Table 2 shows the comparison of the propagation delay obtained from the delay analysis done on each power supply.

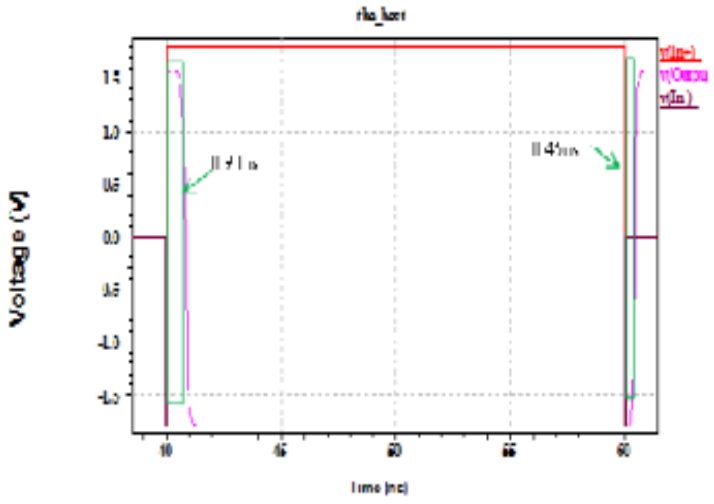

Fig. 7. The output waveform when power supply is 2.0V

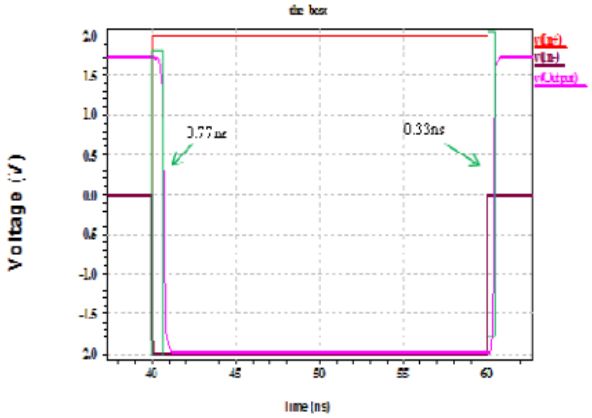

Fig. 8. The output waveform when power supply is 1.8V

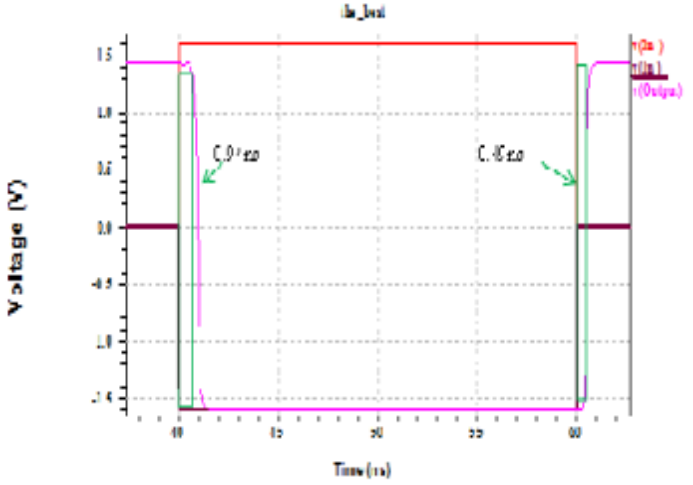

Fig. 9. The output waveform when power supply is 1.6V

Table 2. Comparison of the propagation delay using different supply voltage

Power supply (V)	Output		Propagation delay (ns)
	tplh (ns)	tphl (ns)	
2.0	0.33	0.77	0.550
1.8	0.45	0.90	0.675
1.6	0.49	0.94	0.715

As expected, it is found that a higher power supply voltage will result in a smaller delay time as shown in Figure 7.

7. POWER ANALYSIS

The power (P) drawn from the power supply is proportional to the supply current and the supply voltage. From Table 3, it is found that the power dissipation is least when the power supply used is 1.6V. As expected, the value is higher when a higher power supply is used.

Table 3. Power dissipation of comparator with different power supply

Power supply (V)	Power dissipation (mW)
2.0	1.4709
1.8	1.2293
1.6	0.7899

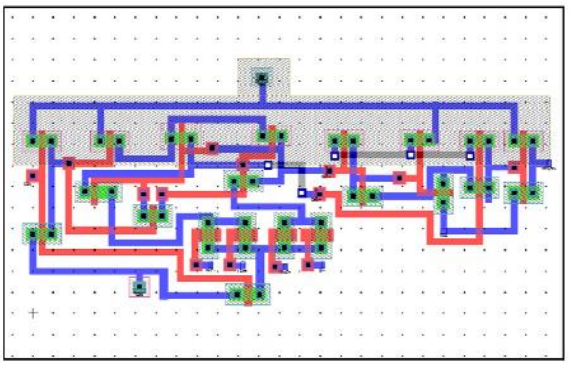

Fig 10. Layout of dynamic latch comparator

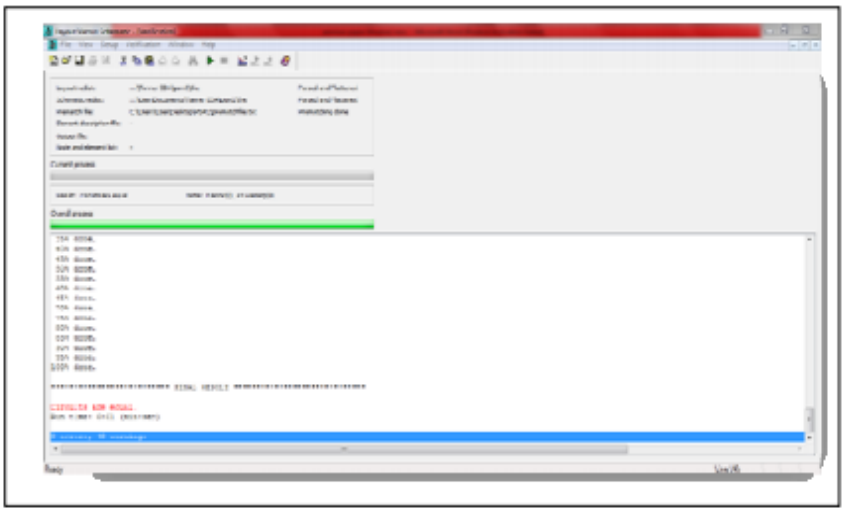

Fig. 10. LVS result

8. LAYOUT OF THE COMPARATOR

The layout of the complete low power dynamic latch comparator circuit using 0.25 μm is shown in Figure 10. This layout minimizes the area by sharing the drain and source connections between MOSFETs. By doing so, the final area size for the circuit is very small and compact. Figure 11 shows the layout versus schematic (LVS) result. The LVS result verified that the layout and the schematic circuit are equal.

9. CONCLUSION

The speed and the power consumption of the comparator have important influences on the performance of ADC. Both are equally important, but usually user cannot get these two parameters hand in hand. It is found from this research that the power dissipation is least with a 1.6V power supply, however the propagation delay is longer as compared to the other two power supplies. On the other hand, the 2.0V supply resulted in the highest power dissipation of 1.471mW but with the shortest propagation delay of 0.550ns. In conclusion, one has to compromise between power dissipation and the speed. Further research and modification will be done on the circuit to lower the power consumption as the overall result of the power dissipation is slightly off than the targeted value.

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