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Design of a Power Efficient Comparator by Using Domino Logic

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ABSTRACT

The implementation of 4 bit comparator circuit using Domino Logic (High speed Domino) and CMOS Logic. The CMOS Logic during inverter circuit operation when voltage level shifts from high to low and vice versa short circuit current occurs which leads to power loss. So this is one of the power saving technique which helps to avoid this short circuit current and saves power consumption. So we have made a comparative analysis between the Domino logic and the CMOS logic for which we have used comparator as our reference circuit. The parameter which we have considered in this paper is power. We also tried to fetch power consumption at different voltage level (voltage scaling) and at least 55% of power is saved by Domino Logic as compared to that of CMOS circuits. In this paper 0.25µm technology is used. And LTSPICE is used to implement the circuit for simulation result.

Keywords: Comparator, Domino logic and Power Consumption.

1. INTRODUCTION

The problem with CMOS circuits is power loss during its operation. This power loss is mostly because of the short circuit current occurs during the switching of voltage level high to low and vice versa. This short circuit current occurs for small amount of time and when the supply voltage $V_{dd\ or}$ V_s meets the Ground during switching period of voltage. As this switching state is not able to specify any logic level and hence the current which flows through the circuit is not of any use. So because of unnecessary flow of current leads to power loss and this is unwanted. Hence the current which is generated during short circuit is called as short circuit current. That is the main drawback of circuits which are implemented using CMOS logic. So to get rid of this short circuit current and power loss we can use such logic which is capable of saving power by removing the short circuit current effect. So we can go for Domino Logic which can fulfil the criteria of power saving. In this paper we have used high speed domino technology which is one of the types of Domino technology Domino logic works in two phases as we can see in Fig. 1 i.e. precharge phase and evaluation phase. For this precharge transistor and evaluation transistors are used.

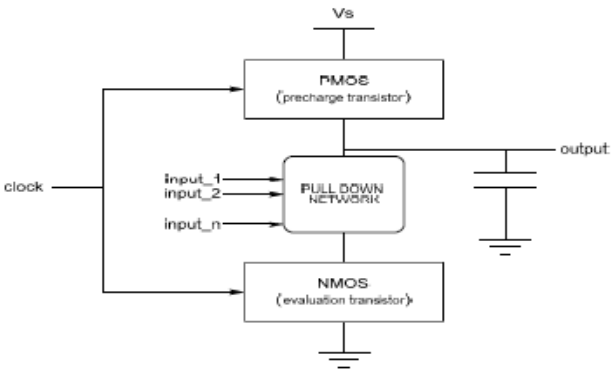

Fig. 1. Block diagram of Domino Logic

The Precharge transistor is PMOS which connects pull down network to the main supply V_{dd} and evaluation transistor is NMOS which connects pull down network to the ground. In precharge phase circuit makes itself ready

for the operation and in evaluation phase the evaluation of final results will be there which will generate appropriate outputs. So in Domino logic there is no chance that the V_{dd} and ground can create short circuit even for small amount of time because they are working in two different phases.

Domino logic is a type of Dynamic logic which require clock for its proper functioning. During negative clock cycle precharge phase comes into consideration where pull down network will get connected to V_{dd} and capacitor will get charged to the same level to that of $V_{dd\,or}$ V_s. Then at positive clock the time of evaluation phase comes where pull down network will get connected to ground and when functionality of circuit will gets satisfied at that time the capacitor will get discharged through ground. This is how proper output will be generated without any short circuit current and hence the power loss will be much more less than that of CMOS logic circuit. In our case the pull down network is 4 bit comparator circuit.

2. COMPARATOR DESIGN

Comparator is the important role in many central processing units and microprocessors and its main function is to find the logical relationship between two input signals i.e. whether first signal is equal or greater or smaller than the second input signal. Another function of comparator is to find out OOO (out of order) execution. As our main reference circuit is comparator and we have designed the 4 bit comparator using Domino Logic and CMOS logic as well so to implement 4 bit comparator we stared with 1 bit comparator as in 4 bit comparator circuit 1 bit comparator is also required. Fig.3 shows circuit of 1 bit comparator. At the output side we have A=B (A equals to B), A<B (A less than B), A>B (A greater than B). After designing and understanding this one bit comparator in a proper manner we can go for 4 bit comparator directly where four 1 bit comparators will be required to run the circuit in an ideal way.

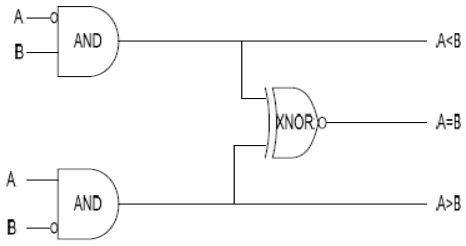

Fig.2. 1 bit comparator circuit

3. 4 BIT CMOS COMPARATOR

As we are implementing this 4 bit comparator circuit using CMOS logic hence there is no need to provide clock to the circuitry. Fig.3. shows CMOS 4 bit comparator. Here we are keeping the W/L ratio 10 which is fixed and number of transistors required are 238. As we can see in the Fig.4 both the inputs A and B are of 4 bits i.e. A3-A0 and B3-B0. As we knows it is an 4 bit comparator hence each input will be of 4 bits and hence A will vary from 0 to 15 which will get compared to B and for simplicity purpose we have assigned a fix value to B i.e. 8(1000) as shown in Table I.

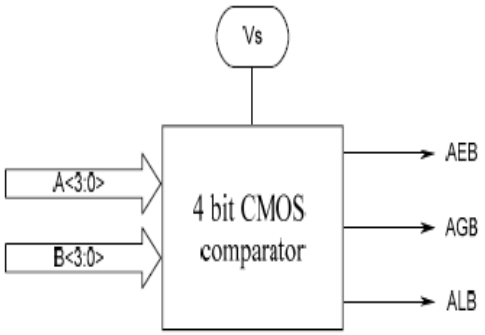

Fig.3. 4 bit CMOS comparator

I also shows truth table for our designed 4 bit comparator and the expected outputs. Now we have used to verify the truth table. Fig. 7 shows the final output waveform where for first eight combinations of A i.e. from 0-7 A is less than B(8). For next sequence A will be equal to B and then for remaining combinations A will be greater than B. we verified those results and it is satisfying the truth table.

Table I. Truth table for 4 bit comparator

A3	A2	A1	A0	B3	B2	B1	B0	AEB	ALB	AGB
0	0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	0	1	0
0	0	1	0	1	0	0	0	0	1	0
0	0	1	1	1	0	0	0	0	1	0
0	1	0	0	1	0	0	0	0	1	0
0	1	0	1	1	0	0	0	0	1	0
0	1	1	0	1	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	1	0
1	0	0	0	1	0	0	0	1	0	0
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	1	0	0	0	0	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	0	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
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1	1	1	1	1	0	0	0	0	0	1

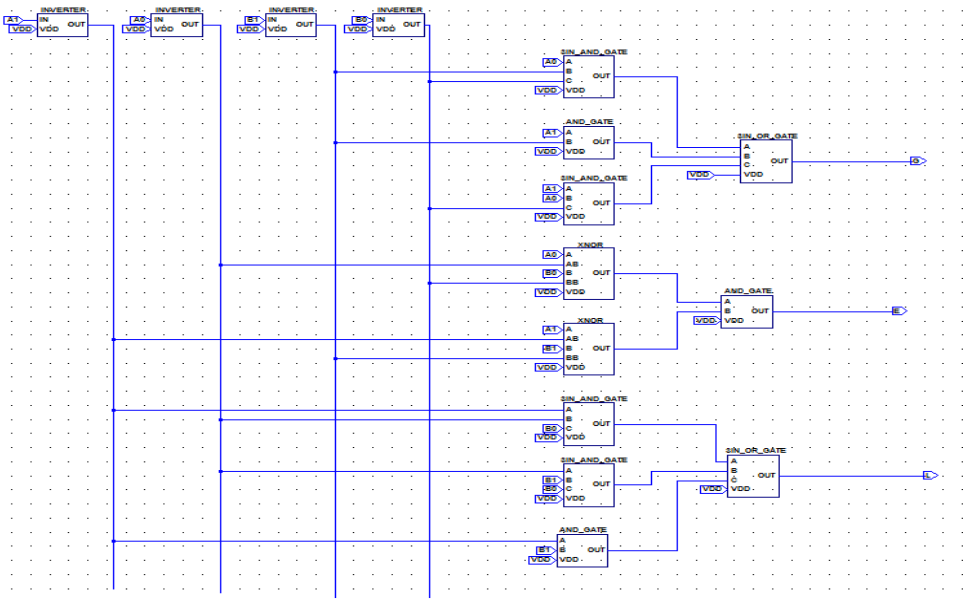

Fig.4. Schematic diagram of conventional 4-bit comparator

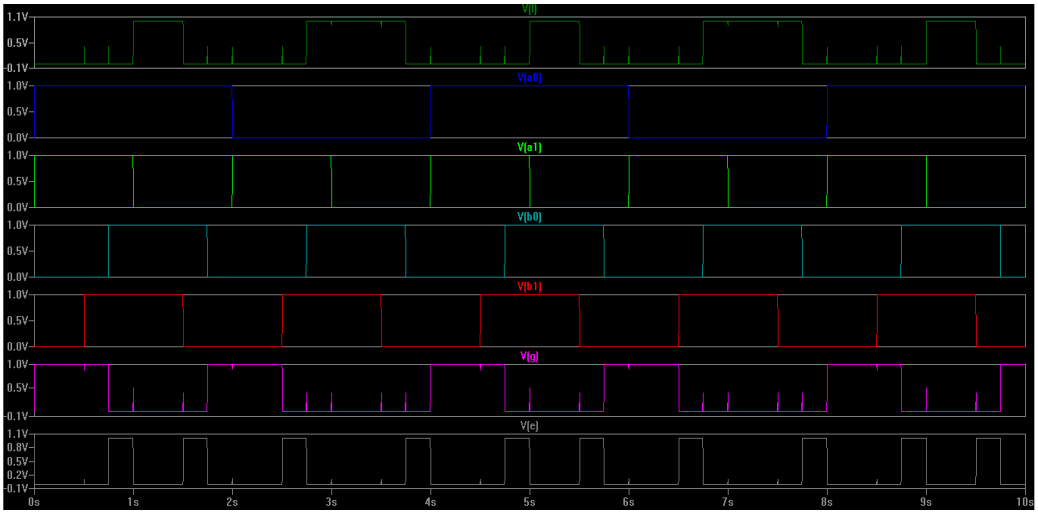

Fig.5 Output waveform of conventional 4-bit comparator

4. 4 BIT HSD COMPARATOR

As we are using Domino logic as the second method with which we are going to design the 4 bit comparator circuit and there are several types of Domino Logic from which we are using High Speed Domino for our operation and the comparative analysis will also in between CMOS comparator and HSD comparator. Here also the W/L ratio will remain same i.e. 10 as in CMOS comparator and number of transistors required are 551. Here we will follow the same truth table given in Table I. Here Fig.5 shows the basic HSD model and Fig. 6 shows the 4 bit HSD comparator.

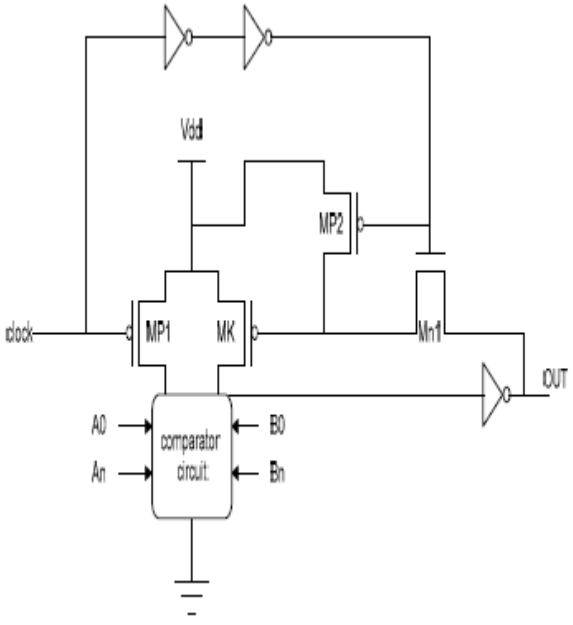

Fig. 6. Basic HSD model

The above circuit is arrangement of high speed Domino Technique which we have used to implement the 4 bit HSD comparator.

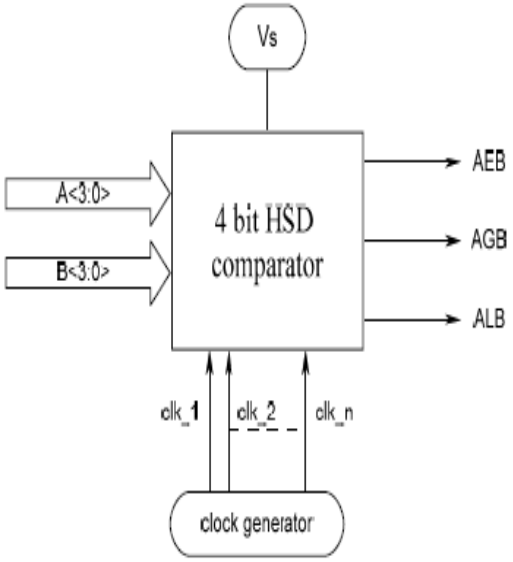

Fig. 7. 4 bit HSD comparator

As we can see in Fig.5. to drive a 4 bit comparator circuit using Domino logic we need a clock generator circuit and n number of clocks where n is number of cascaded stages. we knows that Domino logic generates output only at evaluation phase and hence we can observe the output for only half clock cycle which will be for evaluation phase and for precharge phase circuit will not indicate any output pulse. So we can verify the truth table given in Table I from the output waveform. Shows the output waveform for 4 bit HSD comparator circuit and output waveforms are satisfying the truth table of comparator circuit.

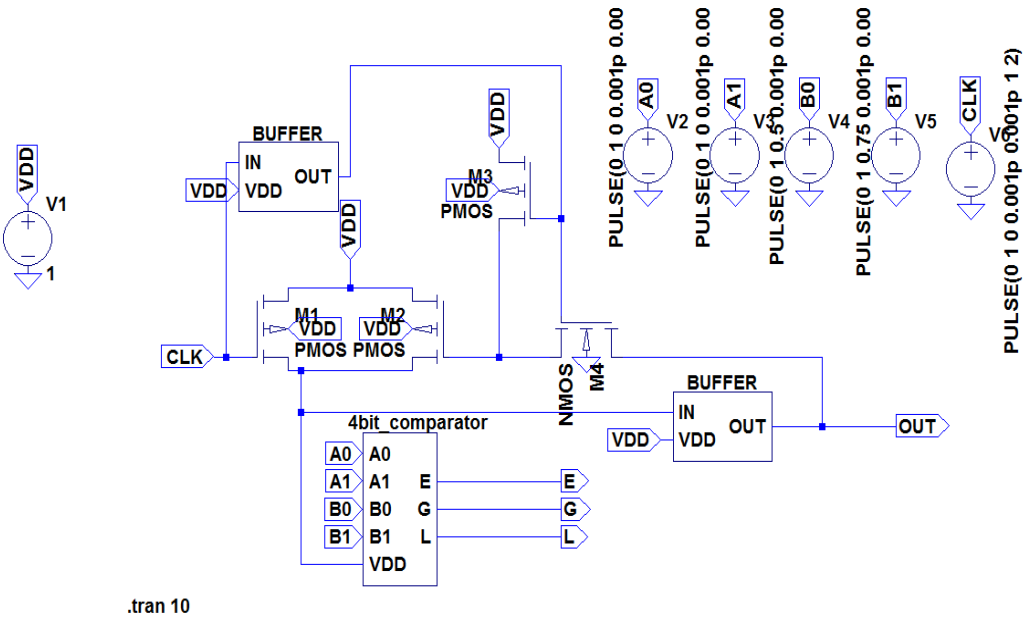

Fig.8.Schematic diagram of conventional 4-bit HSD comparator

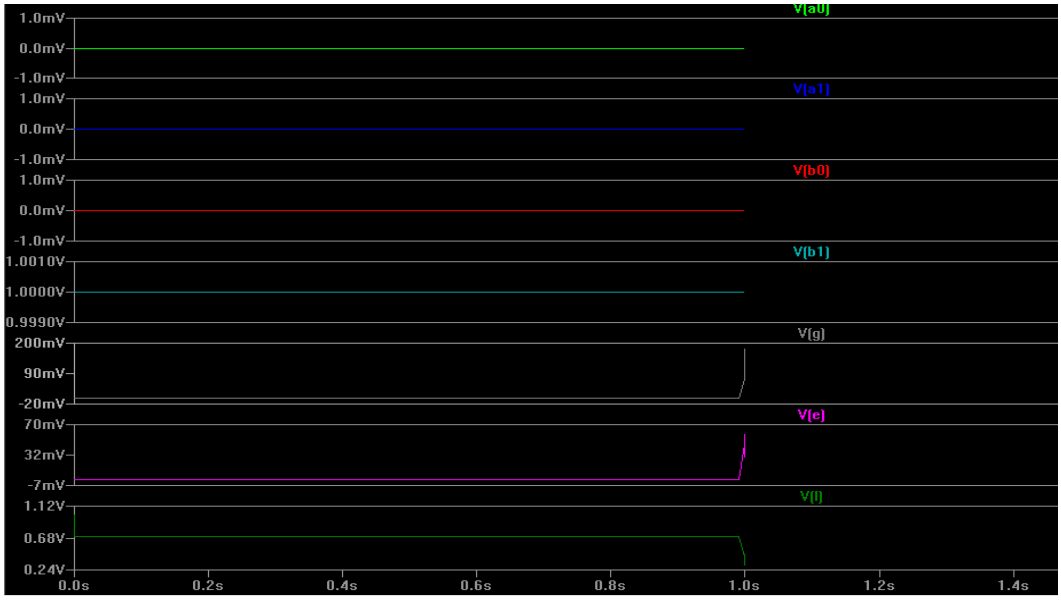

Fig.9 Output waveform of conventional 4-bit HSD comparator

5. RESULT ANALYSIS

Here in this paper we have considered several parameters which we will use for a comparative analysis between the CMOS comparator and the HSD comparator and those parameters are power, frequency, transistors required, voltage scaling and technology Here the technology is fixed which is L=250nm and number of transistors are also fixed which is 238 for CMOS comparator and 551 for HSD comparator. That means now we have to consider the remaining parameters with which we can do the comparative analysis and those parameters are power frequency and voltage scaling.

Table II Power and frequency rating

$V_{dd=}$1V				
L=250nm	**Reference Frequency**	**Power (nw)**	**Maximum frequency**	**Power (nW)**
4 bit CMOS comparator	5MHz	99.308	250MHz	268.100
4 bit HSD comparator	5MHz	26.9506	10MHz	40.4430

6. CONCLUSION

The comparative design and analysis of comparator in both CMOS and HSD domino logic using 0.25µm technology. For comparison we took power, frequency, transistors required, voltage scaling and technology as parameters. We have designed the comparator and verified the truth table using simulation. The domino logic consumes 55% less power than CMOS and the Maximum frequency supported by CMOS comparator is 1GHz

whereas it's 100MHz in Domino comparator and this is the maximum frequency of comparator circuit for CMOS and Domino logic respectively without any optimization for max frequency. For given design Domino logic is better for power saving and CMOS logic is better for high speed operations.

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