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POWER OPTIMIZATION TECHNIQUES FOR HIGH PERFORMANCE 45NM 6T SRAM

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ABSTRACT

The field of digital design aims in designing low power and Optimization-energy driven devices in memories which is useful for portable batteries and numerous emerging applications. Due to high computing capability requirements in battery, SRAM plays an important role to obtain high performance and energy efficiency. In modified 6T-SRAM design provides an approach to reduce power dissipation. The design uses a tail transistor which limits the short circuit power dissipation by interrupting the flow between the supply voltage and ground. By providing stacking effect the tail transistor reduces the subthreshold current, which afterwards reduces the power dissipation. The higher threshold voltage devices are used in the write port for reducing leakage current and lower threshold voltage devices are used in read port for improving high performance. To obtain maximum energy efficient of 6T-SRAM both power reduction and performance improvement are employed in an optimal design. Modified6T-SRAM cell uses single ended read and write operation and have been simulated by 45nm technology using electric tool.

Keywords: Optimization, 6T-SRAM, low power dissipation, high-performance, energy-efficient.

1. INTRODUCTION

Now-a-days to reduce area and to achieve high-performance, energy efficiency the devices are scaled down to great extends. In general, supply voltage is scaled down to reduce power dissipation and the threshold voltage is scaled down to obtain higher performance and energy efficiency in 6T-SRAM. To improve energy efficiency the operating voltage is positioned near or below threshold voltage. In digital design the technology scaling with its reduction in supply and threshold voltages and deterioration transistor off current causes the standby power of the memory to rise [7]. The trend of scaling of device sizes, very low threshold voltage and ultra-thin gate oxide are challenged by variability issues. These unwanted variations results in excessive subthreshold leakage, reverse diode leakage and power dissipation which affects the stability and energy efficient [8]. In this paper, a modified 6T-SRAM is designed using the optimal architecture with the existing optimization techniques such as leakage suppression technique, technique to reduce the retention current and partitioning the memory. Our modified architectural optimization methodology reduces the power reduction and improves high-performance and energy consumption.

2. EXISTING METHOD OF CONVENTIONAL 6T-SRAM CELL

The Conventional 6T-SRAM shown in the figure 1.1 has combination of six transistors in which four transistorsM1, M2, M3, M4 form back to back connection of inverters to store single bit either ‘0’ or ‘1’. The two transistors M5 and M6 are used as access transistor for write purpose of data form to bitlines. Word Line (WL) is used to turn “ON” and “OFF” the access transistor. BL and BLB are the bitlines [5]. The Conventional 6T-SRAM is not stable for deep nano-scale technologies due to low read static noise margin. There are many configuration proposed for improving the 6T-SRAM stability. The reduced supply voltage in deep submicron technologies which is important to keep both high performance and energy consumption under control.

To reduce the power of SRAM is to reduce supply voltage (Vdd). The way discussed to reduce the device size to nanometer region. The device size is reduced by one-half cuts the gate capacitance by one-fourth which reduces the power dissipation. If it used in nano-scale SRAM in a system the static nose margin is too small due to large variation in threshold voltage. SRAM with a single bit line has a larger static noise margin. Bit line precharge voltage should be lower than supply voltage (V_{dd}) [5].

Read Operation: When M3, M4 is turned "ON" the voltage level of BLB bitline will not show variation, there is no current flow through M4, M1 and M3 will conduct o non-zero current. When the voltage level of column BL bit line begins to drop then the voltage V1 (where V1 is the voltage across node 1) will increases from its initial value of 0V. If W/L ratio of access transistor M3 is large to the ratio of M1, the node voltage V1 more than the threshold voltage of M2, it forces an unintended change of the stored data [3].

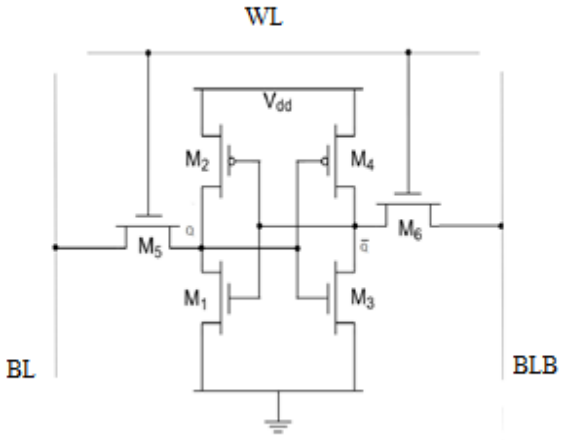


Figure 1.1 Conventional 6T-SRAM Cell.

Write Operation: When the write is '0' operation, assuming initially the logic '1' is stored in the 6T-SRAM cell. The transistors M1 and M6 are turned "OFF", while the transistors M2 and M5 operate in the linear mode. Thus, the internal voltage V1 = V_{dd} and V2 = 0V, the access transistors M3 and M4 are turned "ON". Once the access transistors M3 and M4 are turned on by the row selection circuitry, when node voltage V2 remains below the threshold voltage of M1, then M2 and M4 are designed according to condition. To change stored information V1 = 0V and V2 = V_{dd} the node voltage V1 must be reduced below threshold voltage of M2, so M2 turns "OFF". When V = Threshold Voltage (V_{th}) the transistor M3 operates in the linear region and M5 operates in saturation [3].

3. PROPOSED METHOD OF 6T-SRAM CELL

The proposed 6T-SRAM cell consists of a cross coupled inverter pair (INV1, INV2) connected to a bitline (BL) using access transistor (M5) and a data storage node isolation transistor (M6) is connected to a bitline (BLB). The proposed design is useful for subthreshold SRAM cells without increasing the area overhead and power

consumption. There three control signals used to control write and read operation. The read and write operation access 'n' bit of a word. Therefore, only one read/write assist transistor is required to reduce overhead. In the proposed design the writing/reading of a word is not disturbed when the other word is accessed for writing/reading because a word shares the assist transistor by row not by column. The read assist transistor size is chosen, as it forms critical read access path, which determines the performance. The write assist transistor size is minimized to limit in weakening of cross coupled inverters during write access [5] [6].

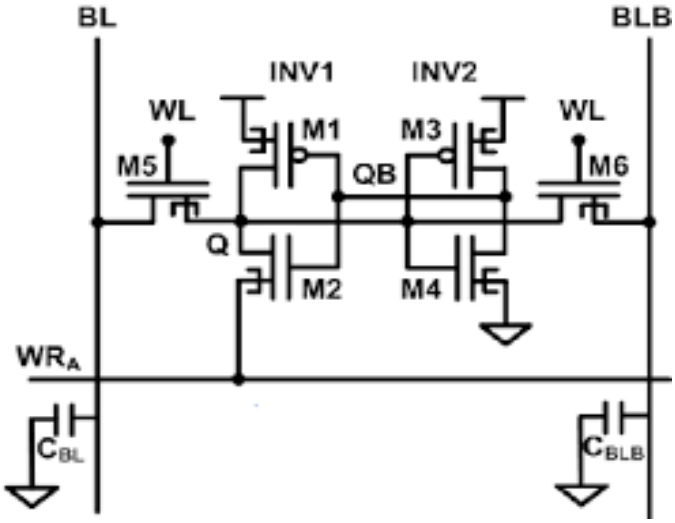


Figure 1.2Proposed 6T-SRAM Cell

Write operation: For write operation in the proposed 6T-SRAM cell, a write assist transistor is used to alleviate the write access problem, which is controlled by control signal for a successful write operation. The write assist transistor is to weaken cross coupled inverters during write access time. The write ability of proposed design at lower V_{dd} is better than the conventional 6T-SRAM cell.

Read Operation: The bitline (BL) is precharged to V_{dd} and read signal is asserted to turn on the read assist transistor which is needed for reading '0'. For reading '1' BL remains at the precharged level because the transistor M6 is turned "OFF". In the proposed design it is importance to notice that to read '0' high to low transition is affected by assist transistor. To read '1' low to high transition is not affected. In this proposed design reading '1' is directly sensed from precharged bitline (BL). In both cases reading '1' or '0' storages nodes are isolated from read current path. The results in proposed design reduced capactively coupled noise due to bitline (BL). It enhances the data stability during read and hold state. In the proposed 6T-SRAM cell the read current path has an equal number of series connected with minimum size features which result in high performance.

4. MODIFIED METHOD OF 6T-SRAM CELL

In the modified 6T-SRAM cell there is one PMOS transistor (PM2) at left node while the inverter on the right side is connected in series with NMOS transistor (NM1), where NM1 is the tail transistor. This tail transistor is used to

reduce short circuit power dissipation. In the modified 6T-SRAM additional signal "cs" is used to control the tail transistor device. The conventional 6T-SRAM structure has two access transistors but the modified 6T-SRAM has one access transistor (NM5) to give write access and other to give read access [6].The working of modified 6T-SRAM consists of three parts such as hold, read and write operation. These operations are explained as follows:

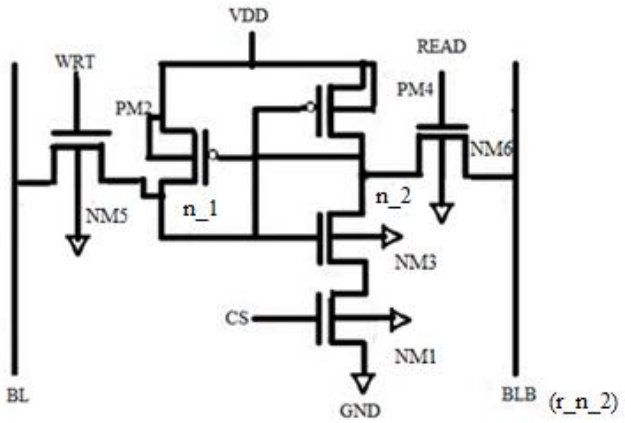


Figure 1.3 Modified 6T-SRAM Cell

Hold Operation: In hold state read and wrt are kept low. If n_1 is holding "0", then NM3 will be "OFF" and PM4 will be "0" then n_2 will be connected to logic high. This is turn will turn "OFF" PM2 which cuts off n_1 from VDD, then "0" is maintained at n_1. Similarly it is done for the case for holding "1".

Read Operation: In the standard operation, bit lines are precharged and the read is given high. During read operation, the internal voltage of the node storing zero arises and may cause flipping of contents of the Conventional 6T-SRAM cell. Due to this data are corrupted. In modified 6T-SRAM the voltage of bit line will not affect the internal node during read operation. A single ended read port is provided for read operation. The bit line is cut-off from the internal node and it is accessed. Hence, the data does not get corrupted. When BL is precharged the wrt is not asserted. Read becomes high and data are stored in n_2 at r_n_2.

Write Operation: In the modified 6T-SRAM only one bitline is precharged to high or low value. If "1" is to be written, BL is charged and wrt is turned "ON". Due to this NM3 also turns "ON", which drains down the voltage at n_2. If "0" is written to n_2 which turns "ON" PM2 and connects to logic high. Hence, "1" is written to node n_1. Likewise "0"n is also written at the node n_1.

5. IMPLEMENTATIO OF 6T-SRAM CELLS

The Conventional 6T-SRAM cell is designed using electric tool and its waveform is simulated is shown below. Similarly proposed 6T-SRAM and its waveform and modified 6T-SRAM cell using Modified 6T-SRAM and its waveform are shown below. Hence I am analyzing the each circuit power consumption and delay.

SCHEMATIC DIAGRAM:

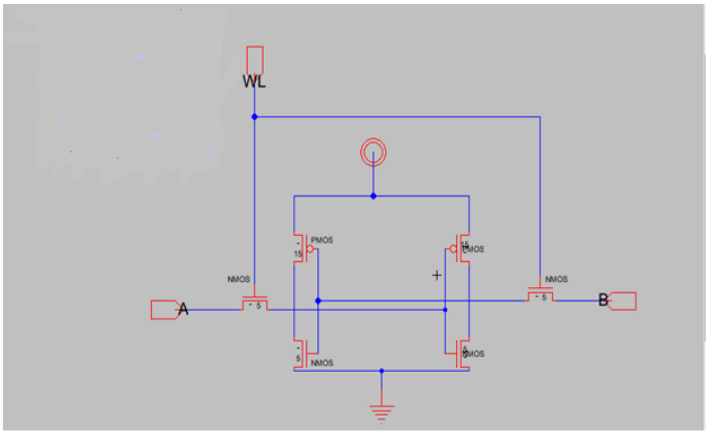


Figure 1.4 Conventional 6T-SRAM Cell

LAYOUT:

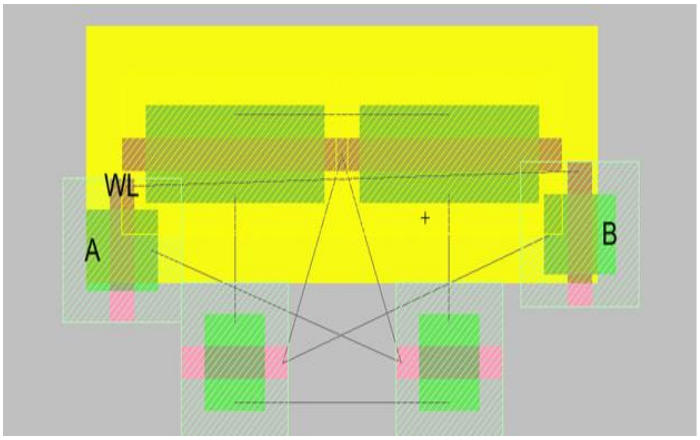
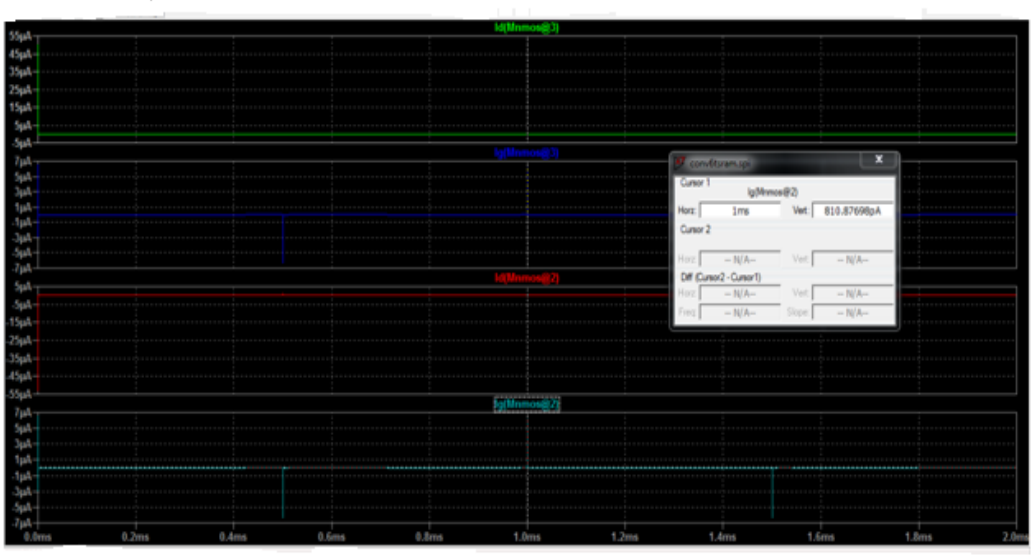


Figure 1.5 Layout of Conventional 6T-SRAM Cell

OUTPUT WAVEFORM:

WL1:



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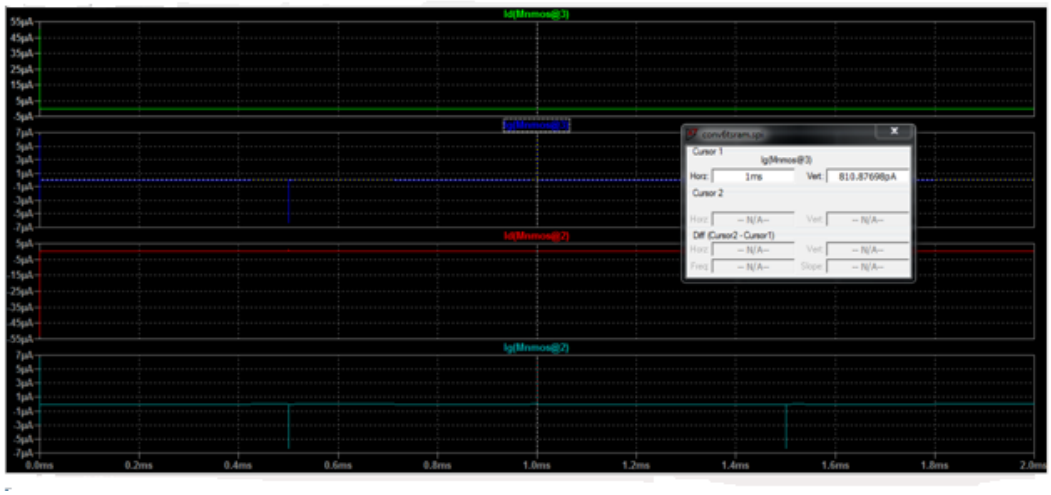
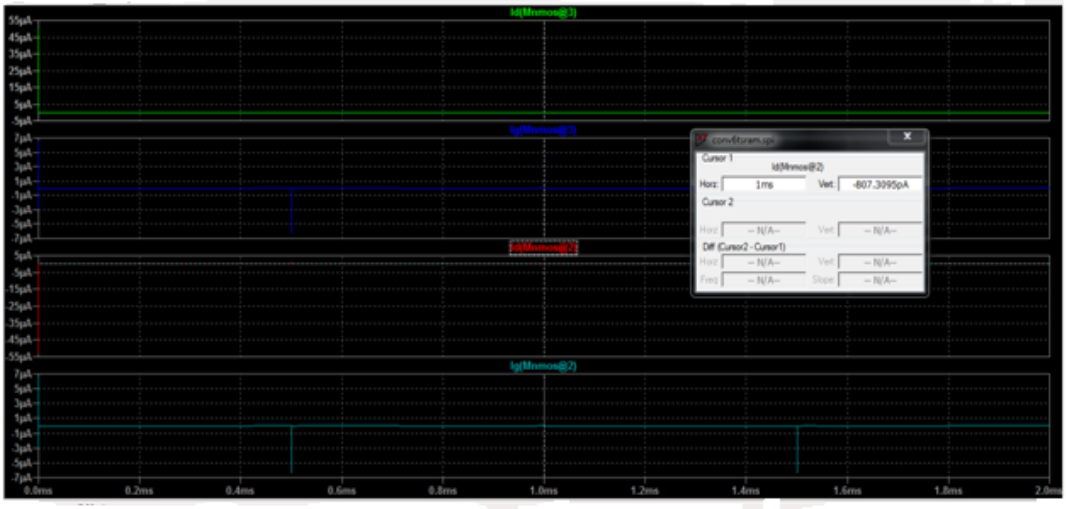
WL2:



A:



B:

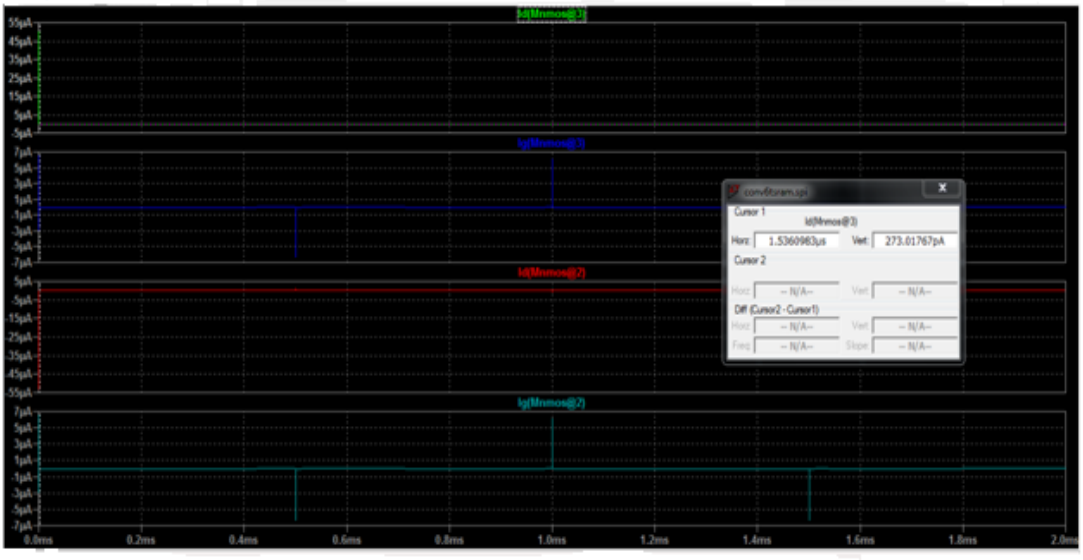


Figure 1.6 Simulation Output Waveforms of Conventional 6T-SRAM

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SCHEMATIC DIAGRAM:

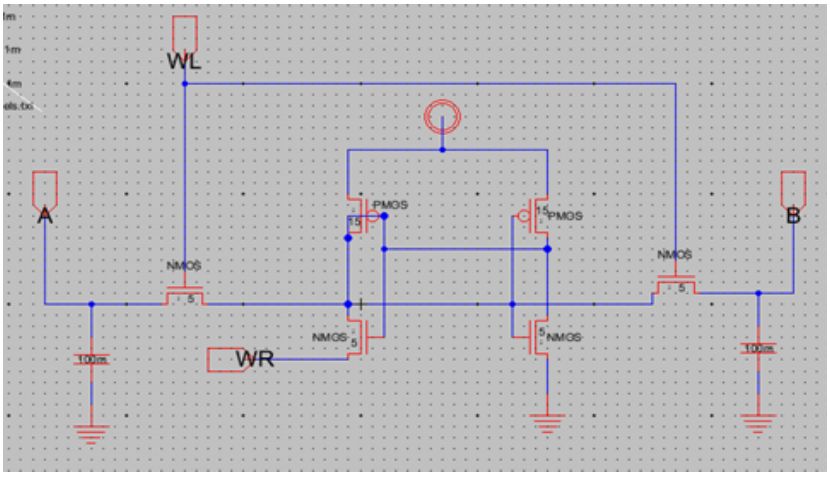


Figure 1.7 Proposed 6T-SRAM Cell

LAYOUT:

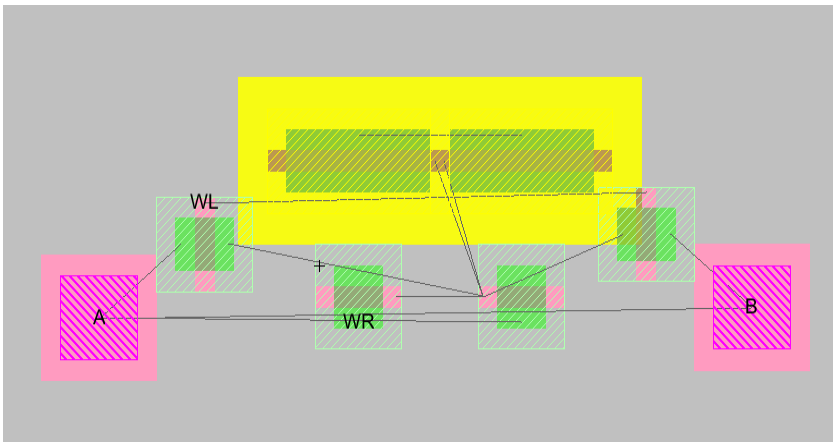
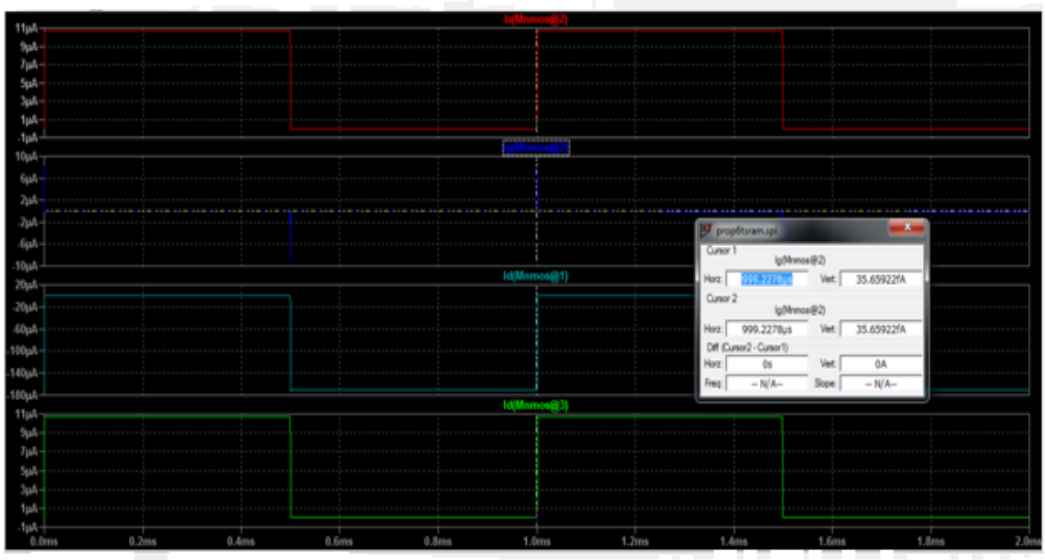


Figure 1.8 Layout of Proposed 6T-SRAM Cell

OUTPUT WAVEFORM:

WL:



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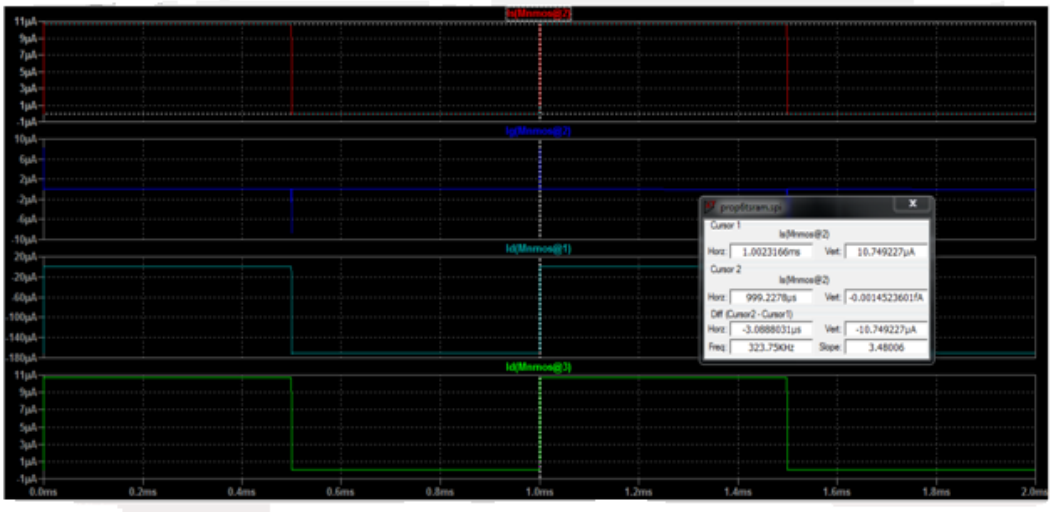
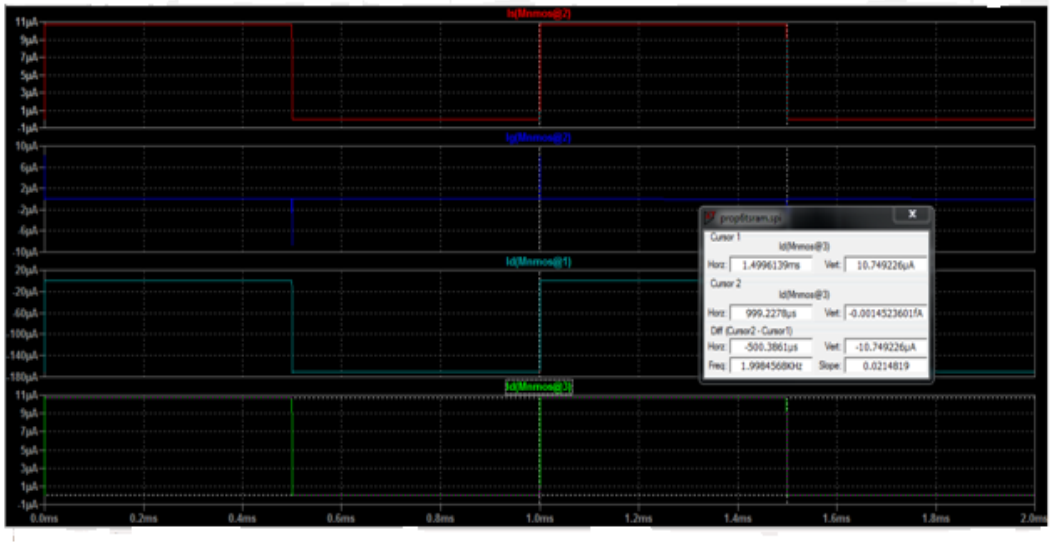
A:



B:



WR:

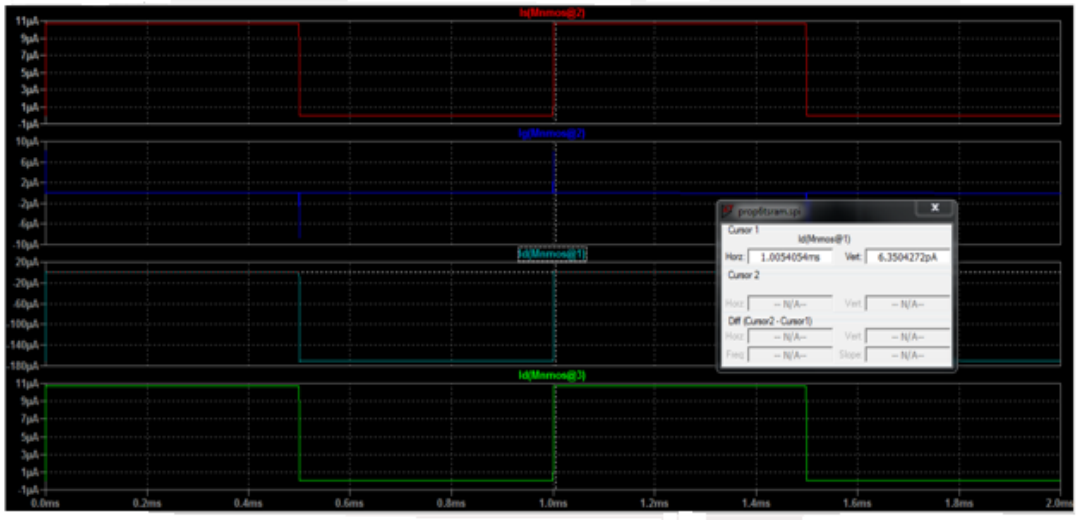


Figure 1.9 Simulation Output Waveforms of proposed 6T-SRAM Cell

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SCHEMATIC DIAGRAM:

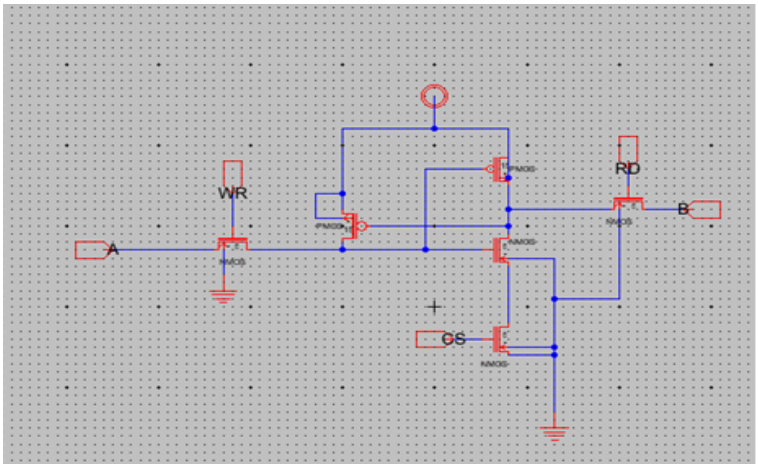


Figure 2.0 Modified 6T-SRAM Cell

LAYOUT:

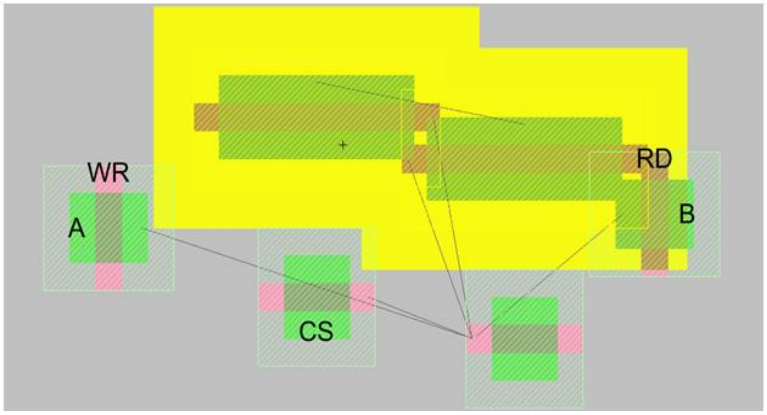
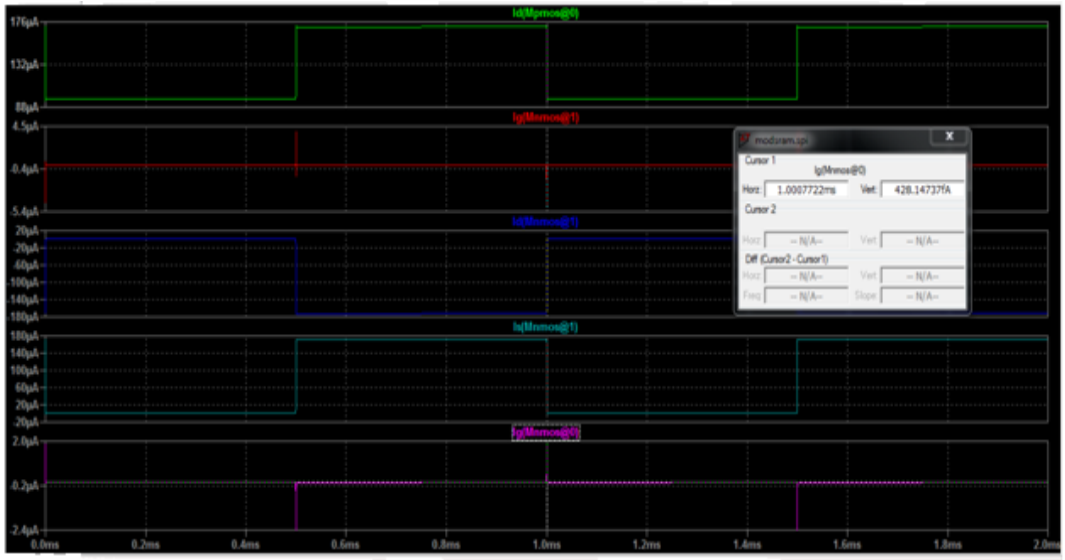


Figure 2.1 Layout of Modified 6T-SRAM Cell

OUTPUT WAVEFORM:

WR:



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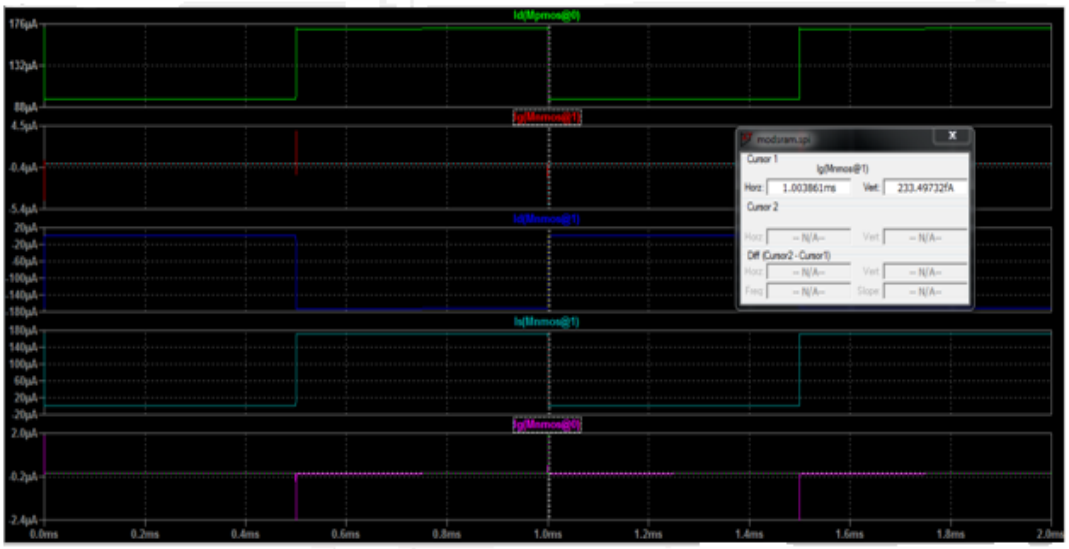
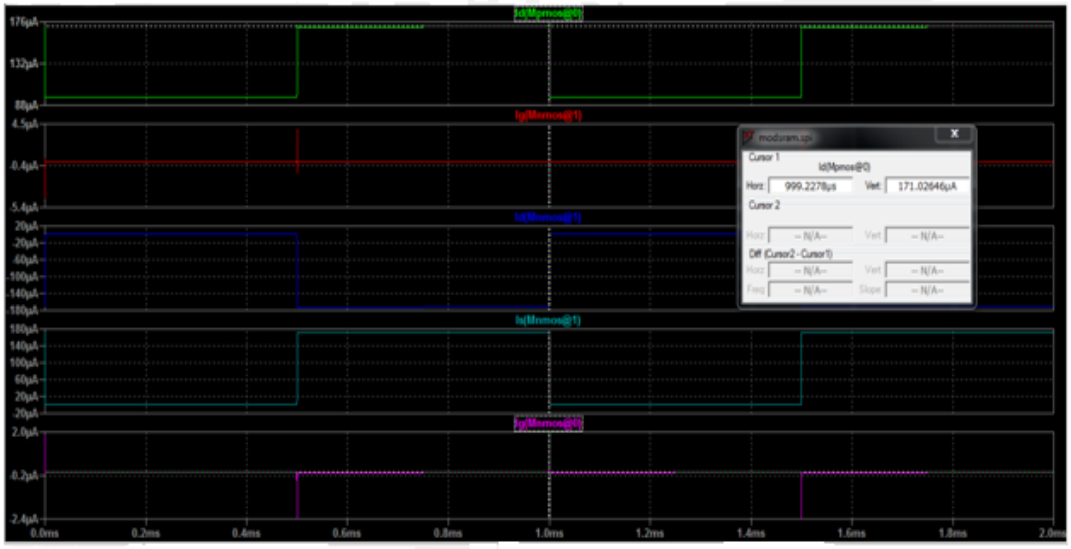
RD:



CS:



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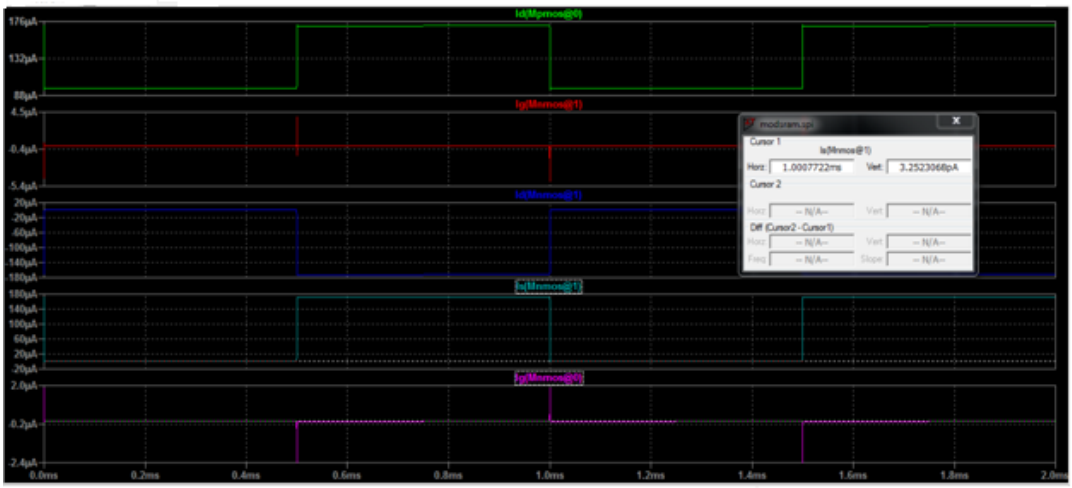

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B:

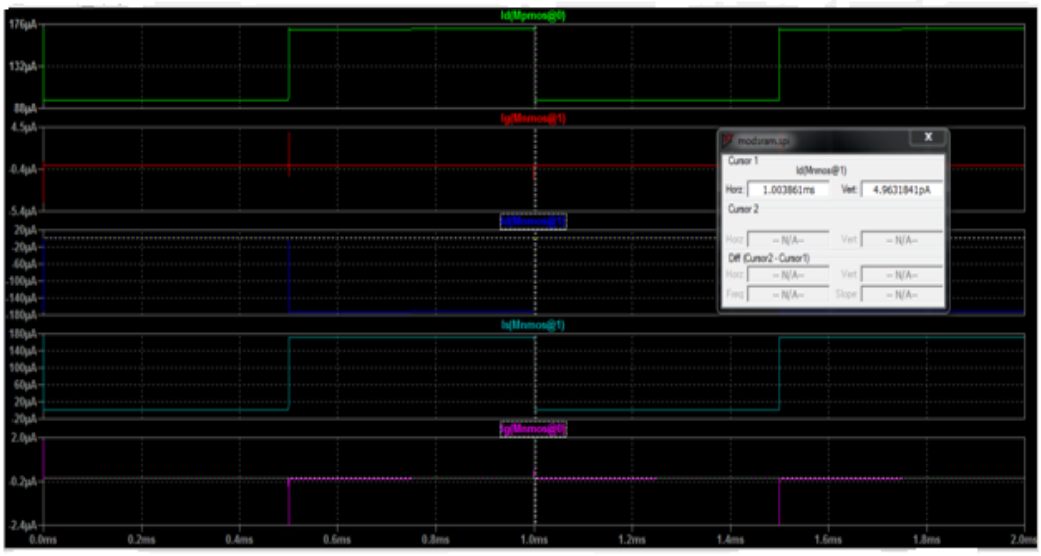

Figure 2.1 Simulation Output Waveforms of Modified 6T-SRAM Cell

6. RESULTS

This paper concentrates on optimizing the power reduction and to obtain high-performance and energy efficiency and to overcome the difficulties in designing SRAM memories. The difficulty arises due to scaling of device sizes. The reduction in supply voltage, threshold voltages and transistor off-current causes the standby power of the memory to rise [4]. Due to scaling the process variation and variability issues are major challenges to reduce power consumption and achieve high-performance and energy consumption. In the presence of process voltage variation and temperature, this paper aims at optimizing the power consumption to obtain high-performance and energy efficiency.

Table 1 Comparison of 6T-SRAM Cells

6T-SRAM				
Circuit	**Voltage**	**Current**	**Write Power**	**Read Power**
Conventional 6T-SRAM Cell	5V	807.3095pA	4036.5475mW	-
		273.01767pA	-	1365.08835mW
Proposed 6T- SRAM Cell	5V	10.749226µA	53.7461mW	-
		6.3504272pA	-	31.752136mW
Modified 6T- SRAM Cell	5V	3.2523068pA	16.261534mW	-
		4.9631841pA	-	24.8159205mW

7. CONCLUSION

This paper presents a 6T-SRAM cell with very low power consumption and reduces leakage current. The effect of process, supply voltage and temperature (P, V, T) on the high-performance metrics of the modified SRAM cell is studied. Excessively higher threshold voltages in the write paths which lead to slower write speed than read to improve energy efficiency. It is concluded that modified 6T-SRAM can be used in low power applications to obtain high-performance and energy efficiency.

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